CMS Phase I Pixel Module Qualification

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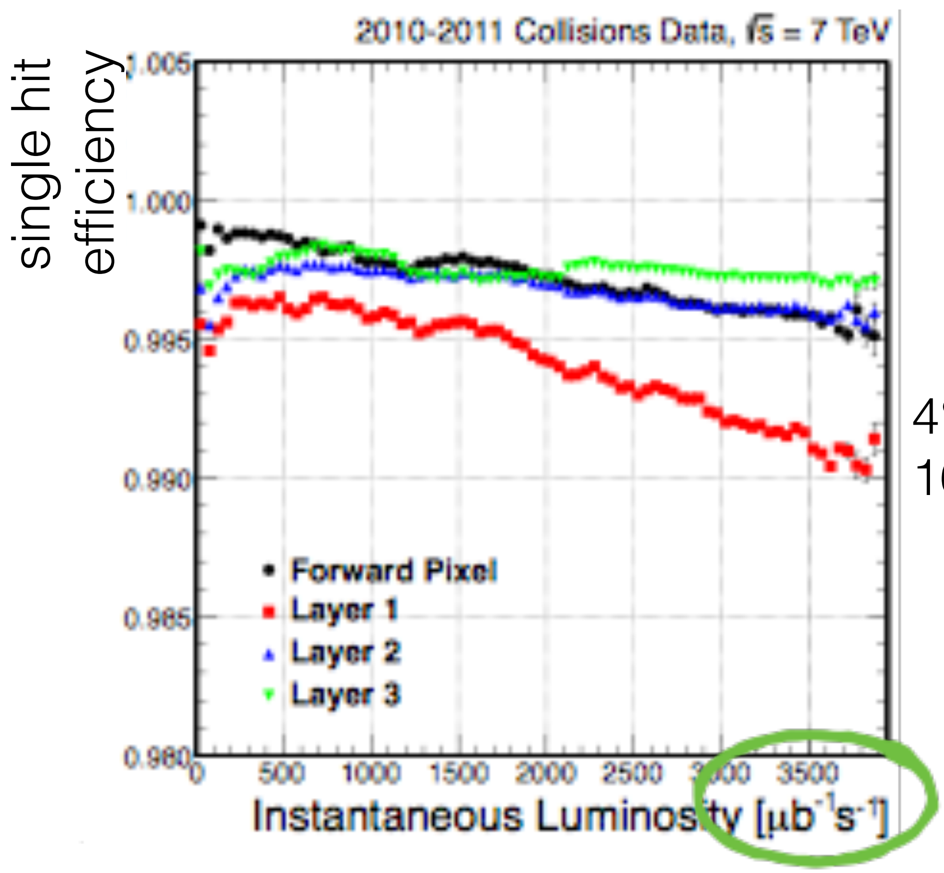
12/12/16

Upgrade Motivation

- LHC has already significantly surpassed design luminosity and continues to increase
- Readout chip buffers are finite
  - Upgrade required to maintain nominal performance

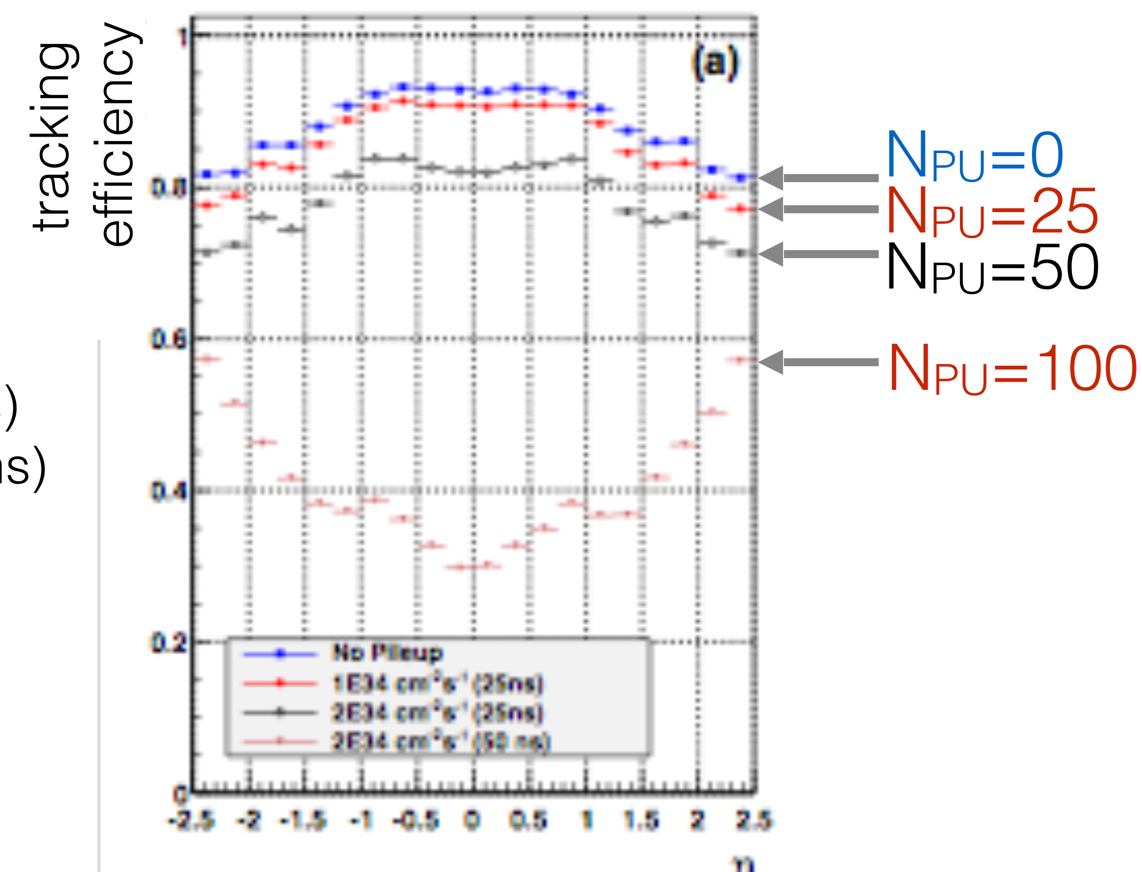
Dynamic inefficiency increases with instantaneous luminosity (pileup)



4% at 1×10^{34} cm^{-2}s^{-1} (25 ns)
16% at 2×10^{34} cm^{-2}s^{-1} (25 ns)

3.5x10^{33} cm^{-2}s^{-1} (50 ns)

Severe degradation of physics performance

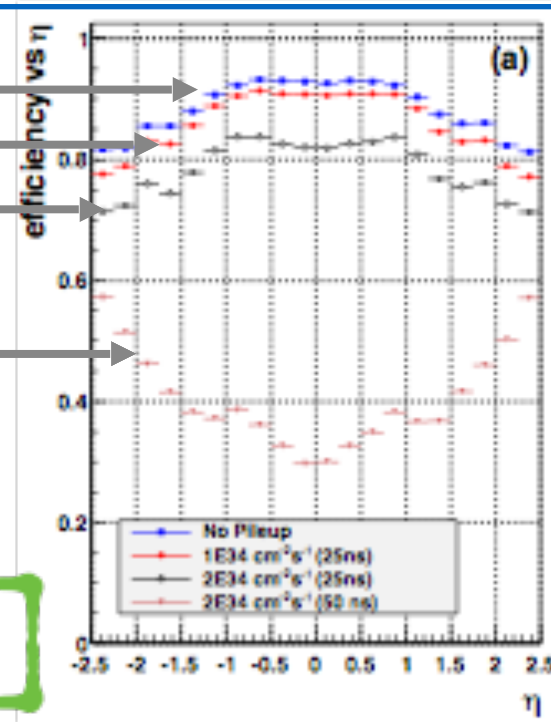


Upgrade Overview

complete replacement of existing pixel detector

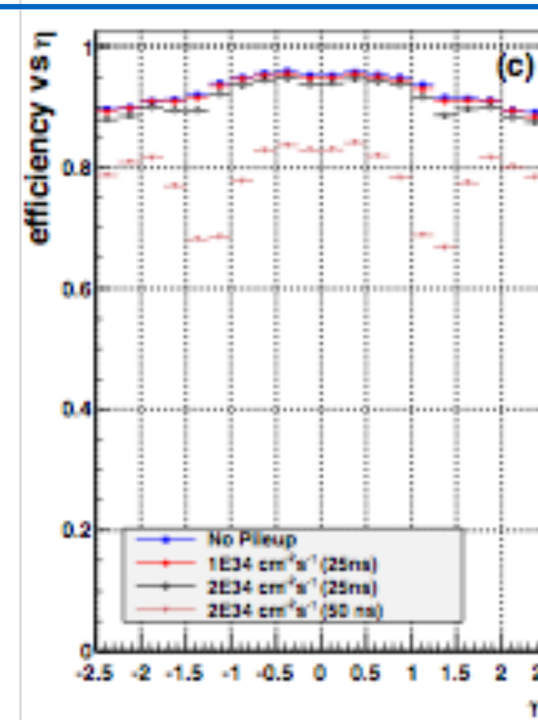
pixel pitch remains 150µm x 100µm

N_{PU}=0
N_{PU}=25
N_{PU}=50
N_{PU}=100



Phase 0

larger buffers
(reduced data loss)



Phase 1

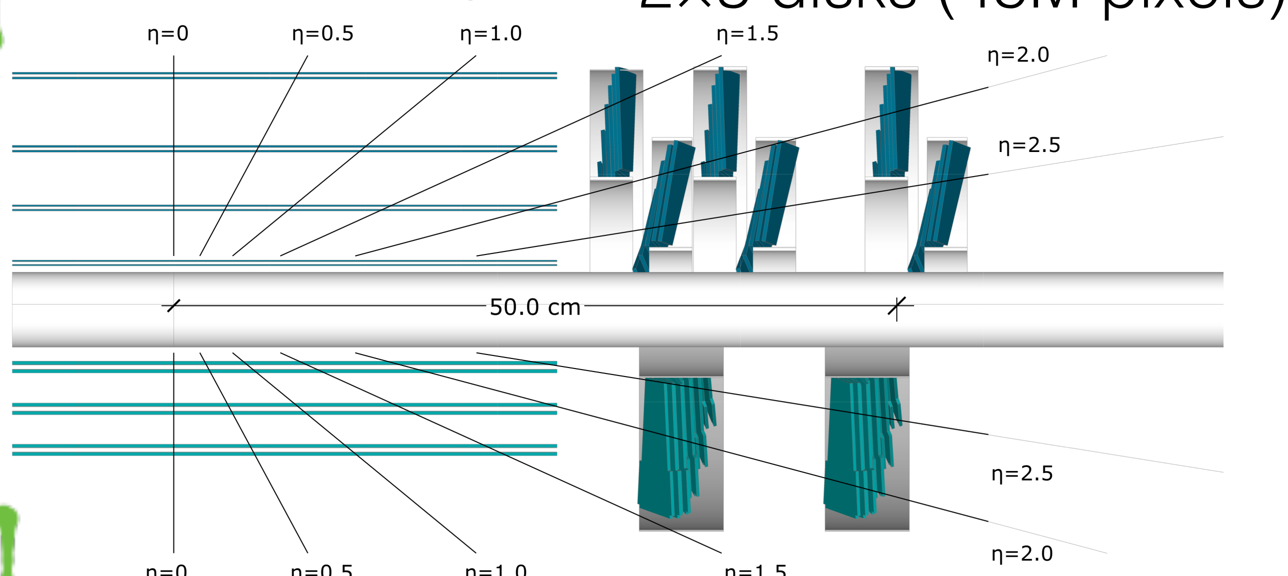
Phase 1

4 hit coverage

2×3 disks (45M pixels)

4 barrel layers

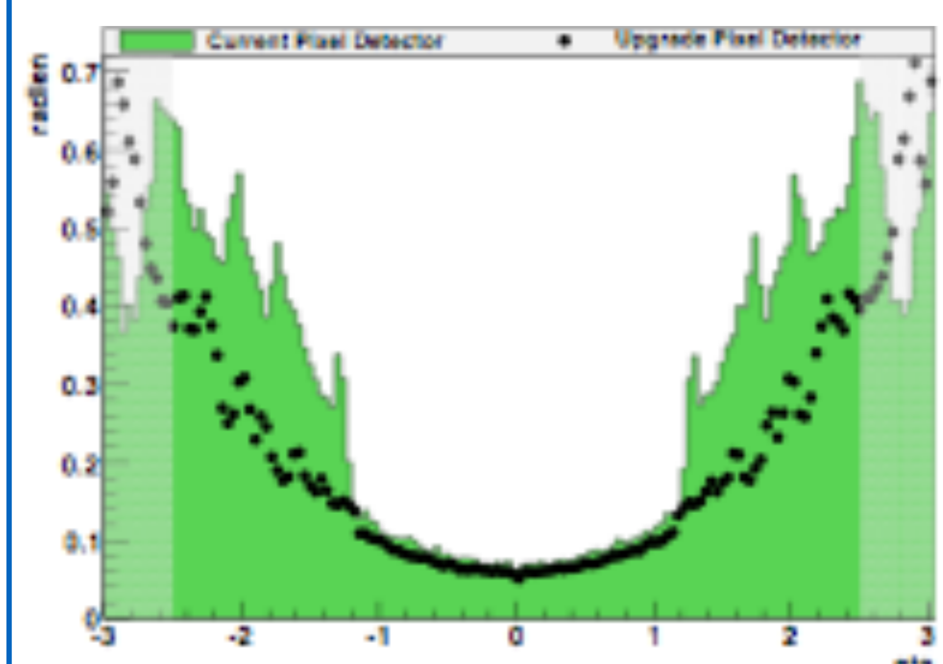
3 barrel layers



Phase 0

2×2 disks (18M pixels)

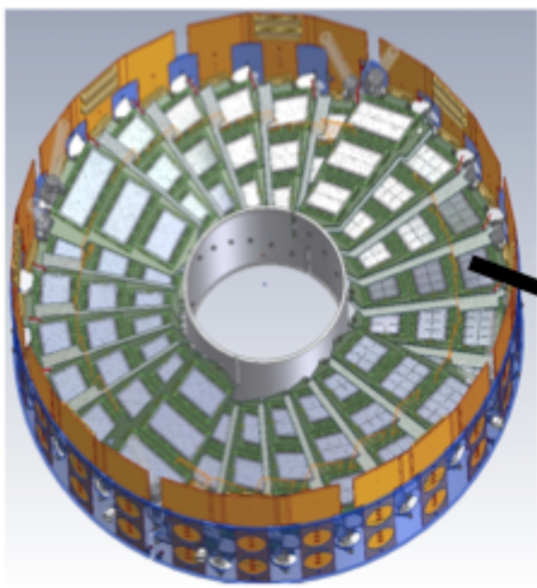
reduced material budget



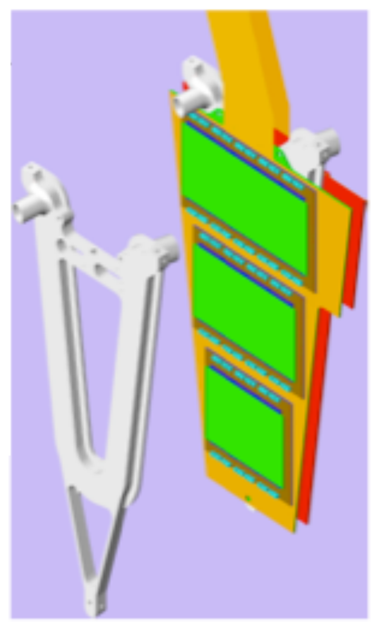
FPIX Disks

Phase 0

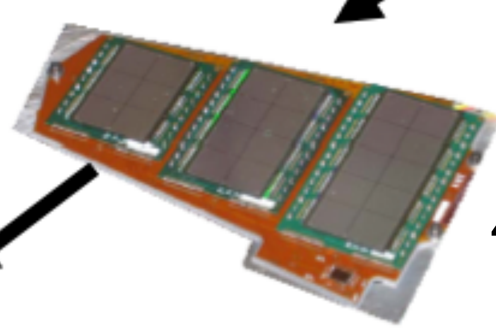
4 disks



blade



panel

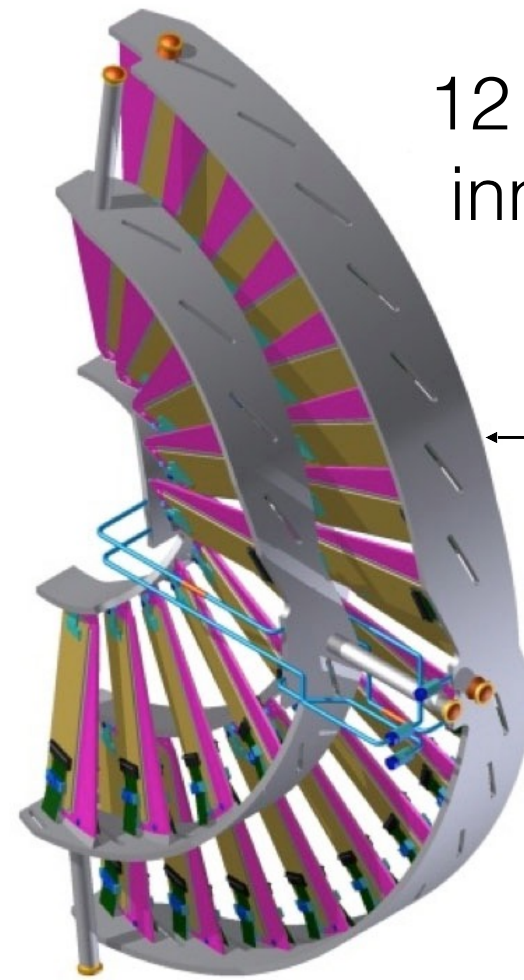


4 types

plaquette

5 types

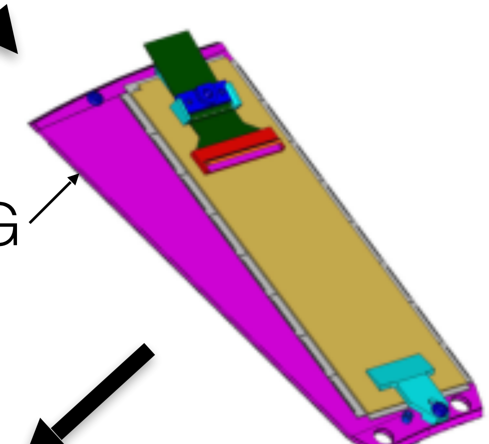
Phase 1



12 half disks (separate inner and outer rings)

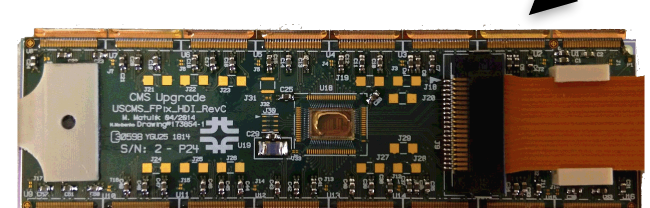
carbon fiber (embedded CO_2 cooling tubes)

outer: 17 blades
inner: 11 blades



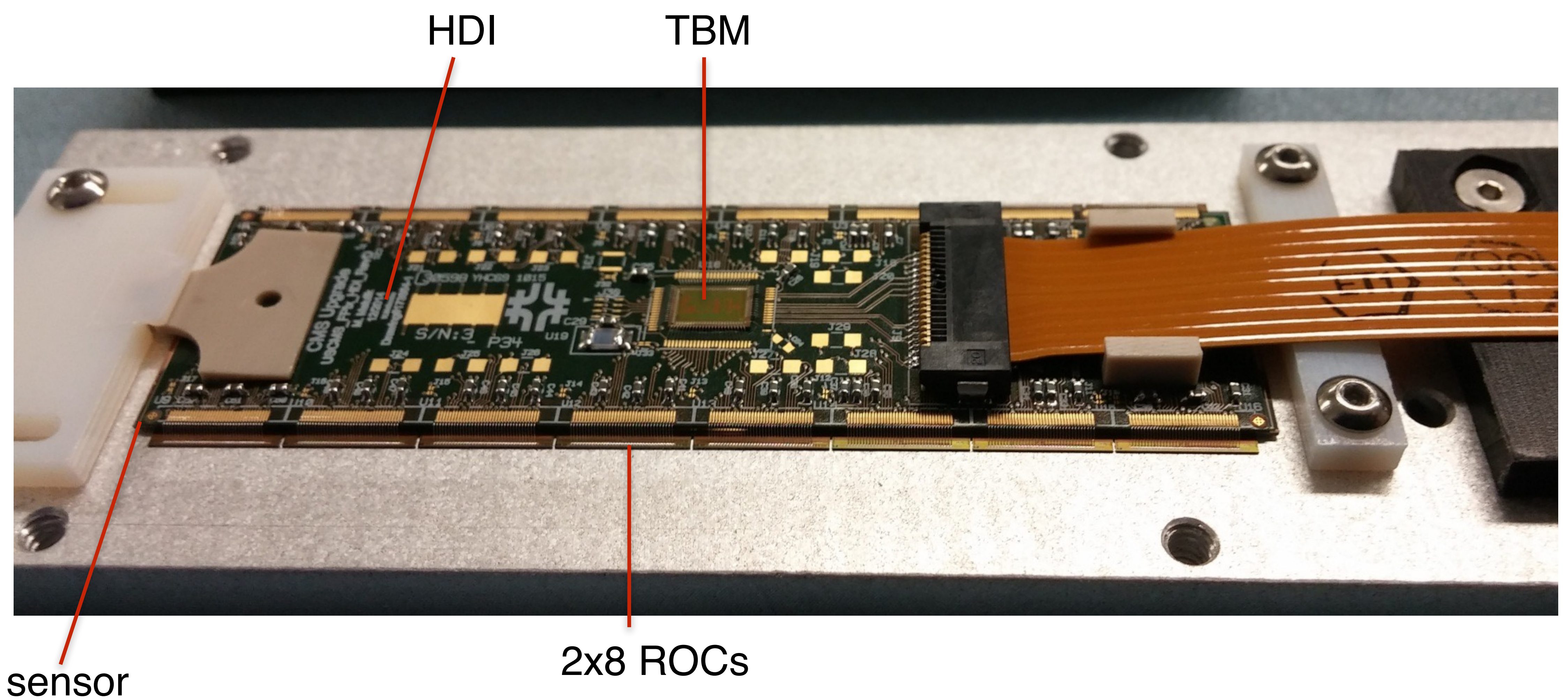
TPG

2x8 module

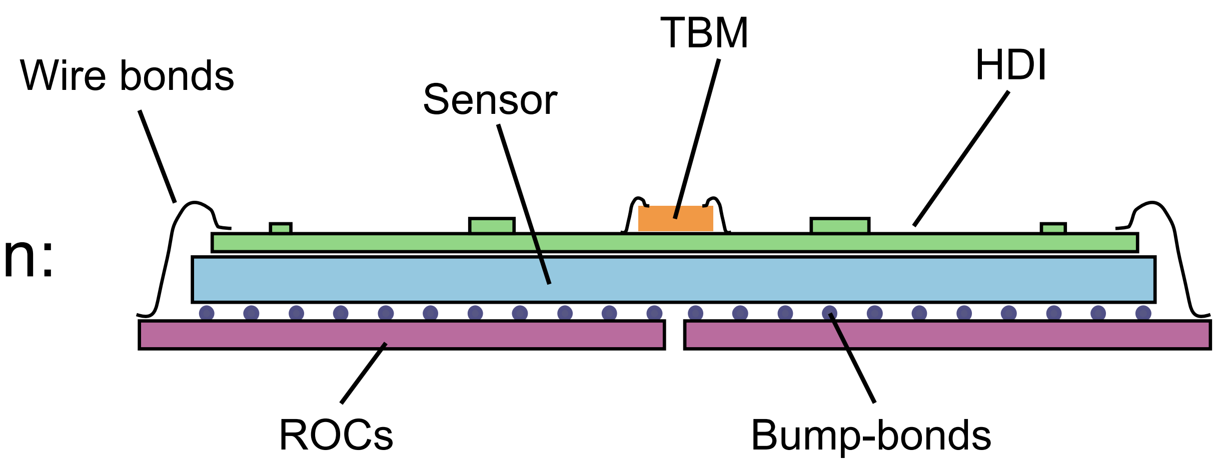


1 type

FPIX Module



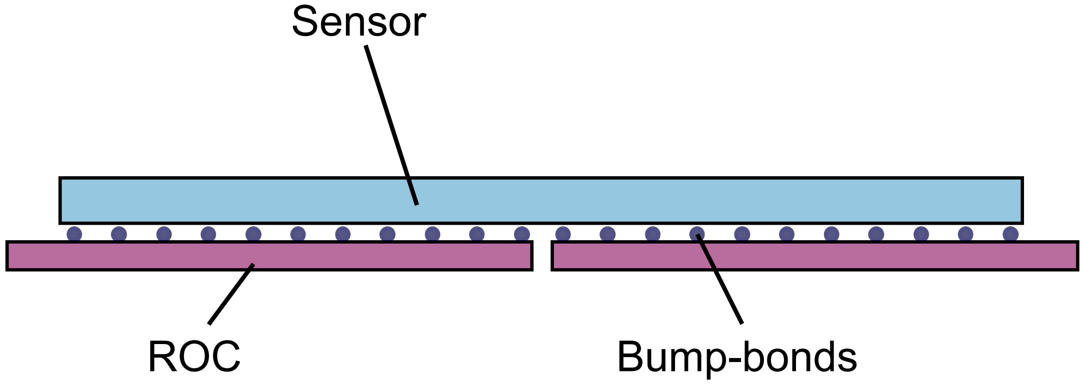
schematic cross section:



66,560 pixels

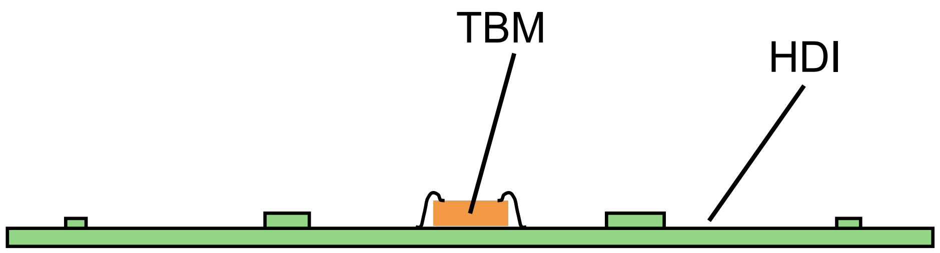
Module Assembly

- Bare module assembly at RTI (~40/week)
  - Dicing ROC wafers
  - Under-bump metallization
  - Bump bonding
  - Flip chip assembly
- Bare modules shipped to Purdue and Nebraska
  - Visual inspection + IV test

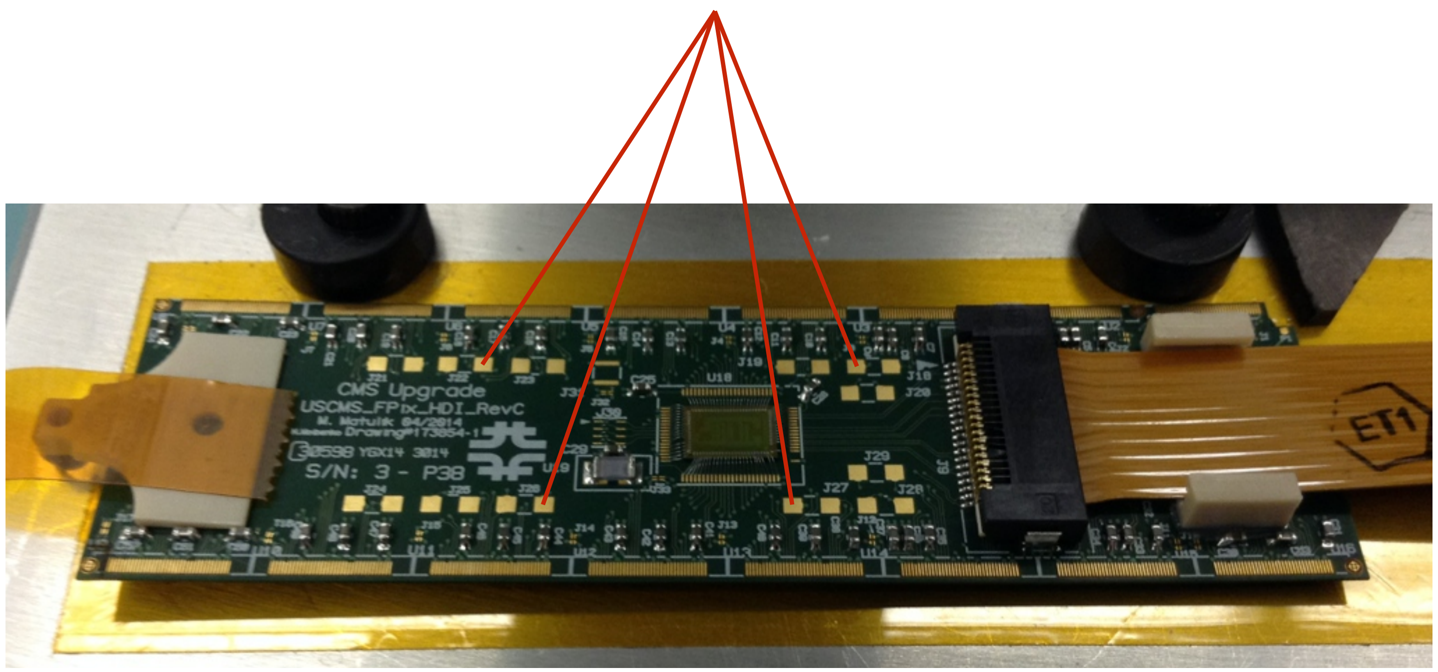


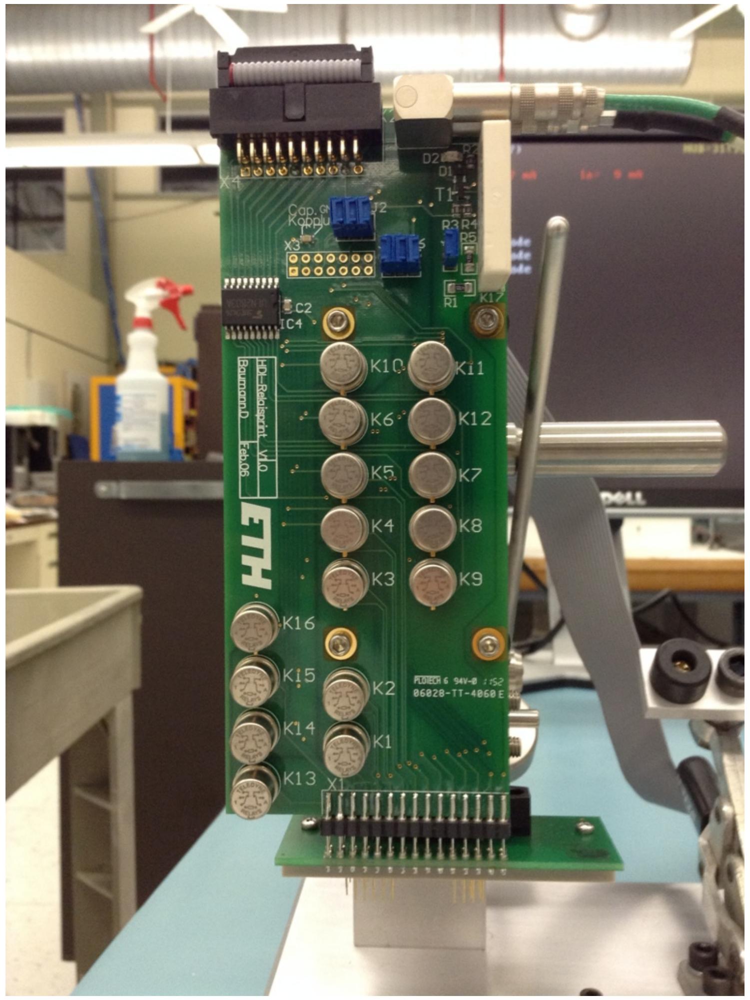
Module Assembly

- Attach surface mounted components and wire bond TBM to HDI at FNAL
- Test TBM functionality with needle card at FNAL



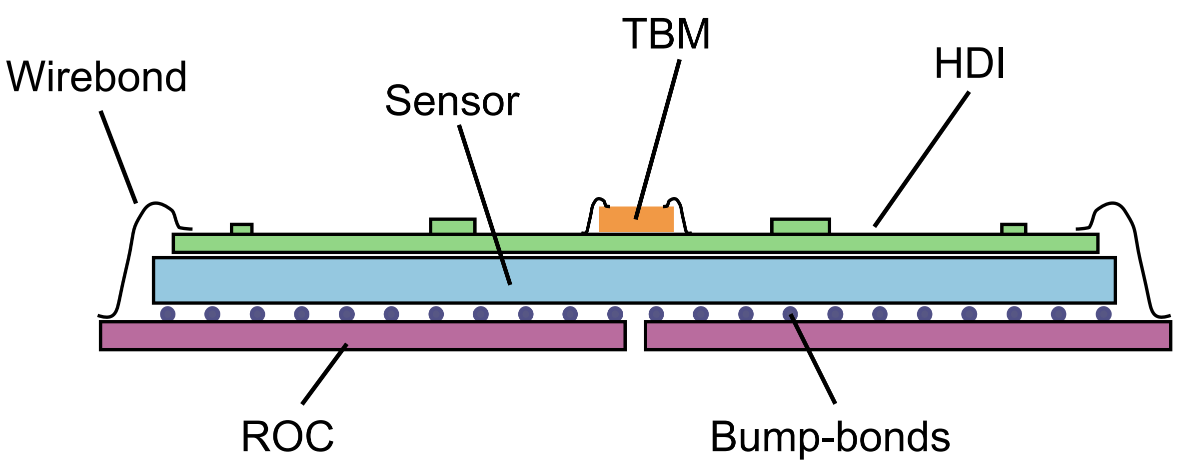
24 probe points

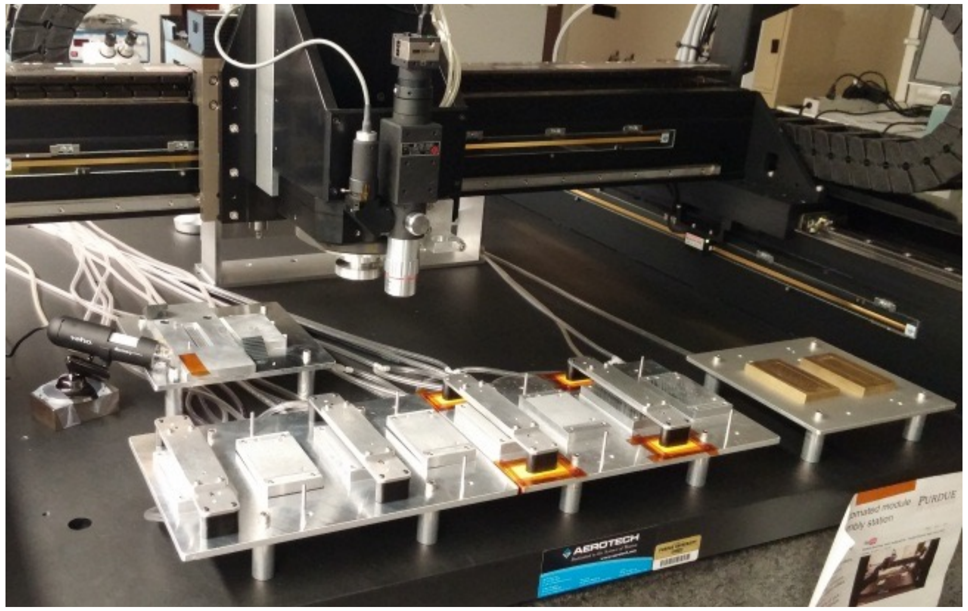




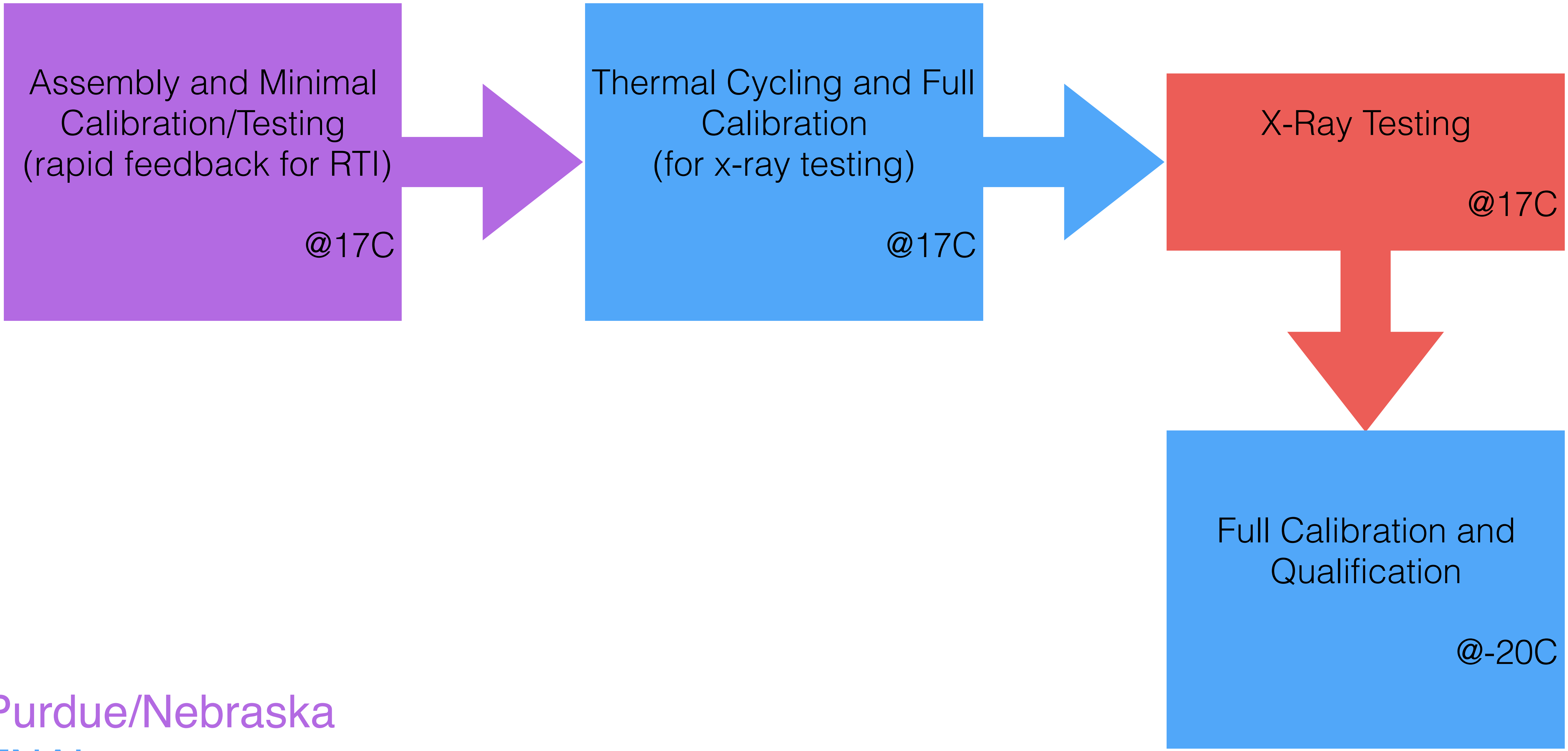
Module Assembly

- Final module assembly performed at Purdue and Nebraska
  - HDI glued to bare module with pick-and-place machine and cured
  - Wire bonding from HDI to ROCs and sensor (HV)
  - Visual inspection + basic module calibration/testing
  - Encapsulation of wire bonds
- Shipped back to FNAL for calibration/qualification





Qualification Workflow



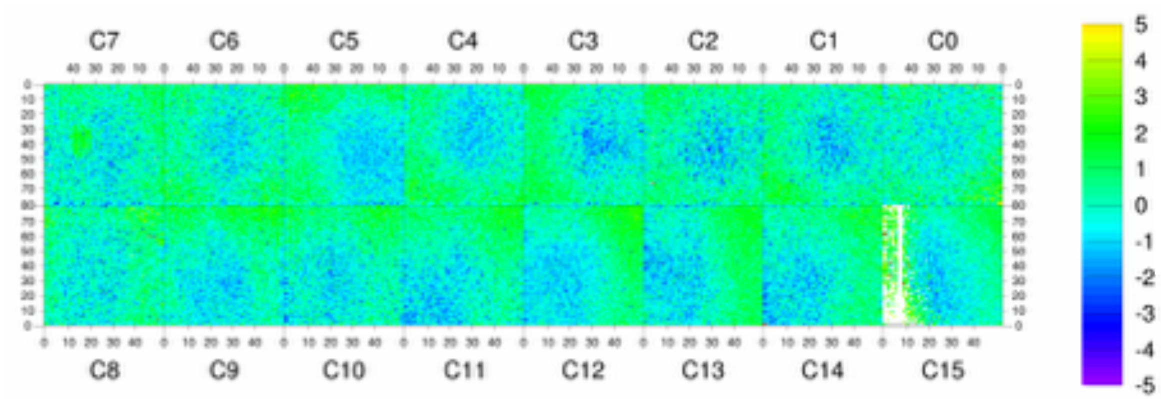
Purdue/Nebraska
FNAL
University of Illinois - Chicago/Kansas

Thermal Cycling

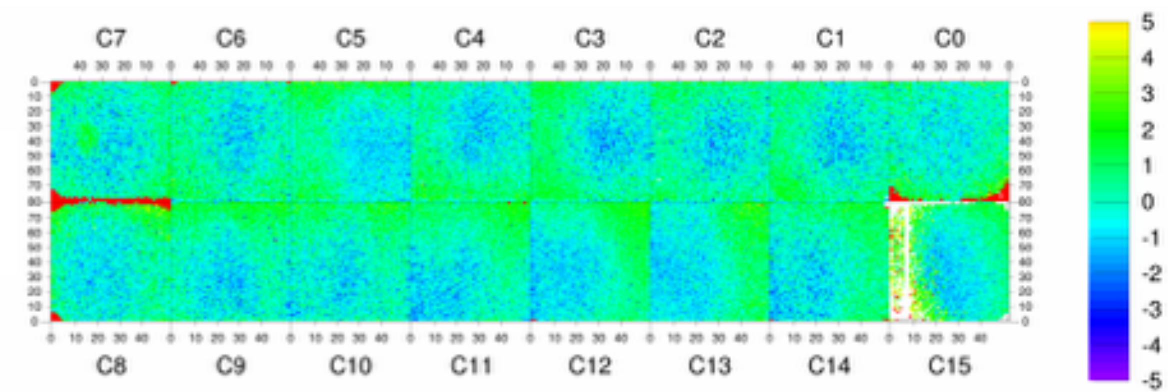
- All modules - 10 cycles between -30C and +50C in a dry environmental chamber
  - Make bump bonds prone to failure fail immediately
- Pet modules - extra cycles:

[Jamie Antonelli]

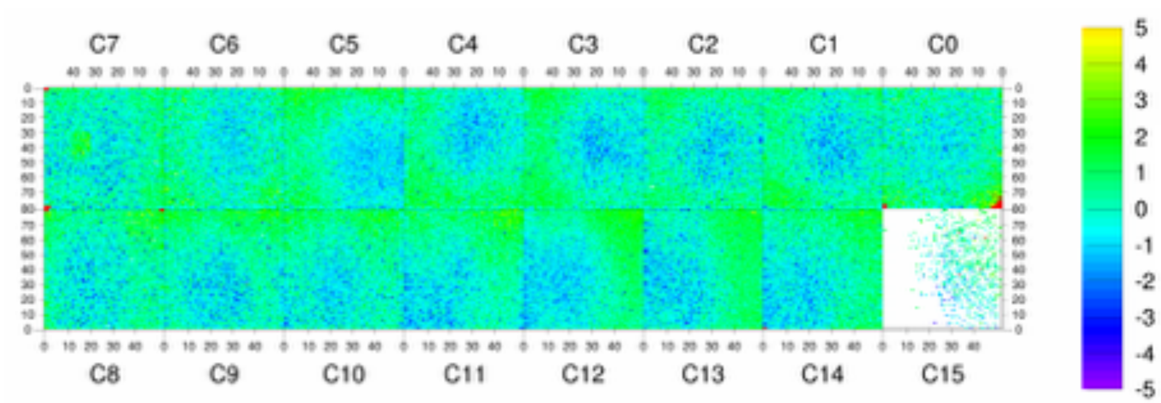
10



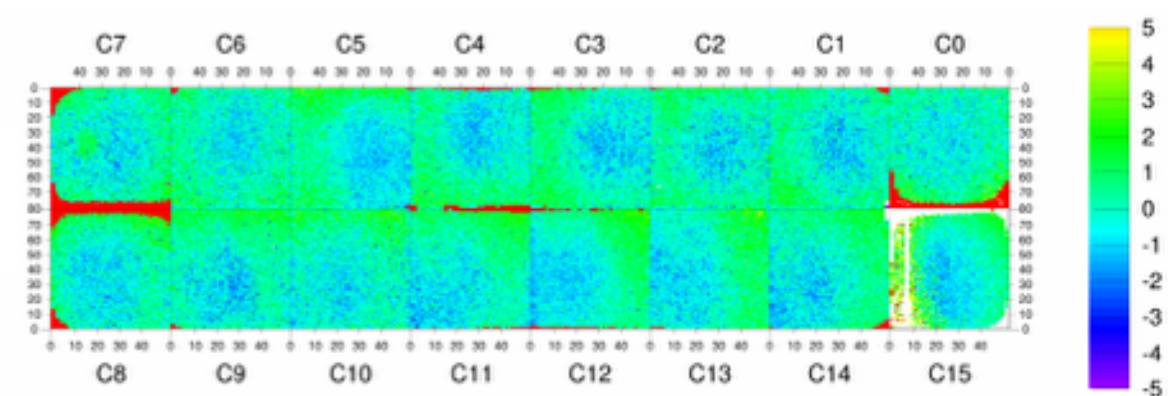
100



50

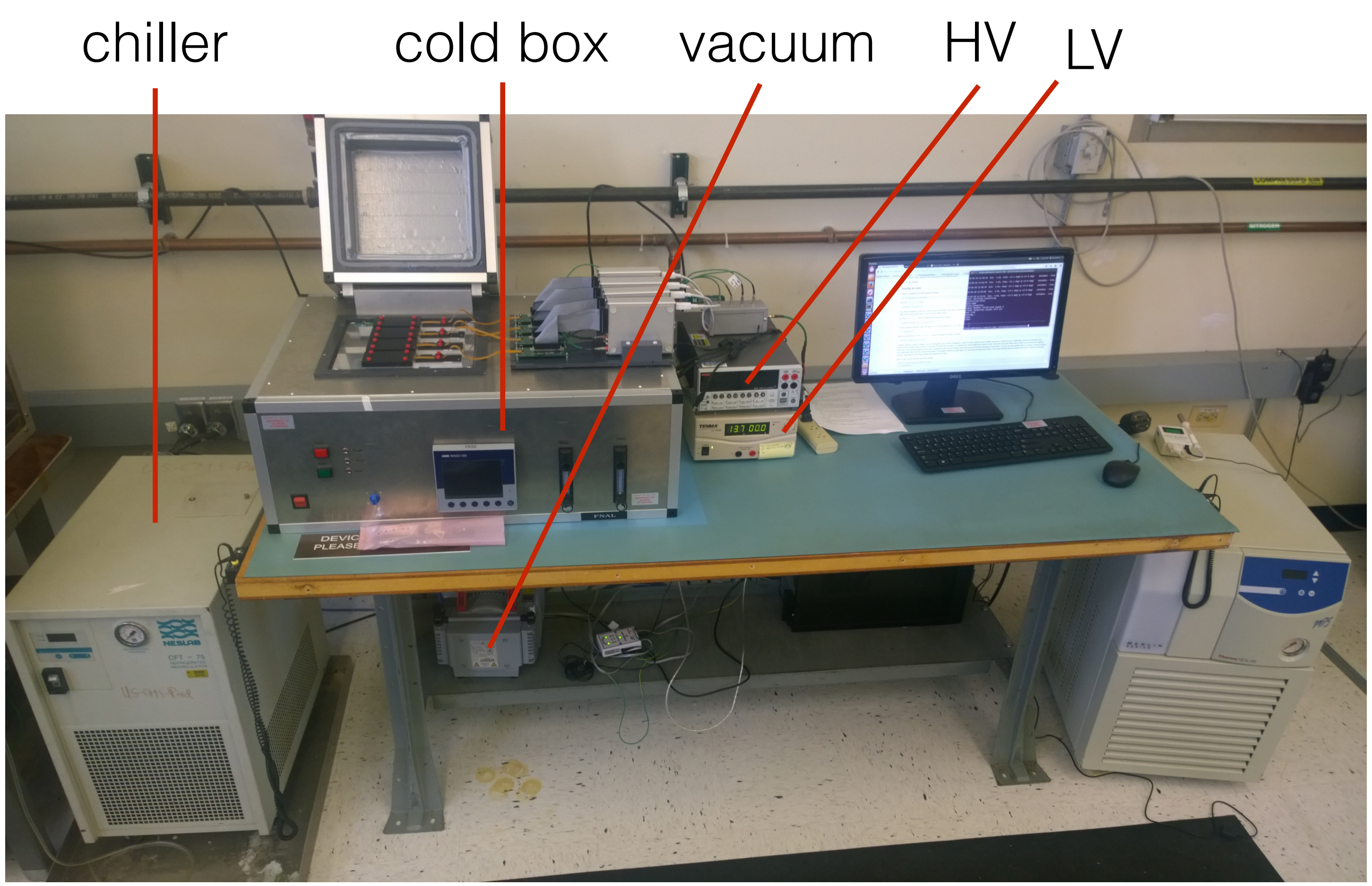


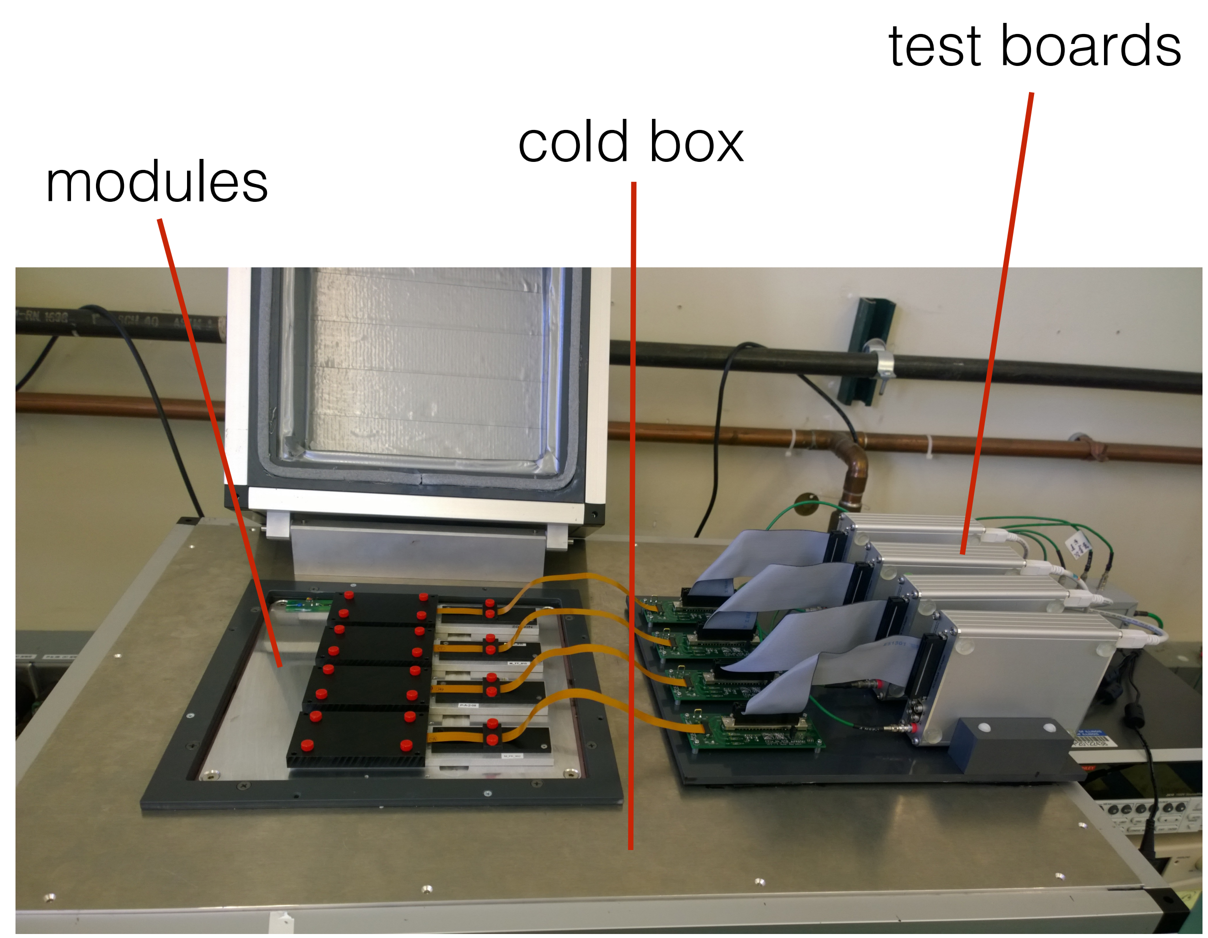
150



FNAL Test Stands

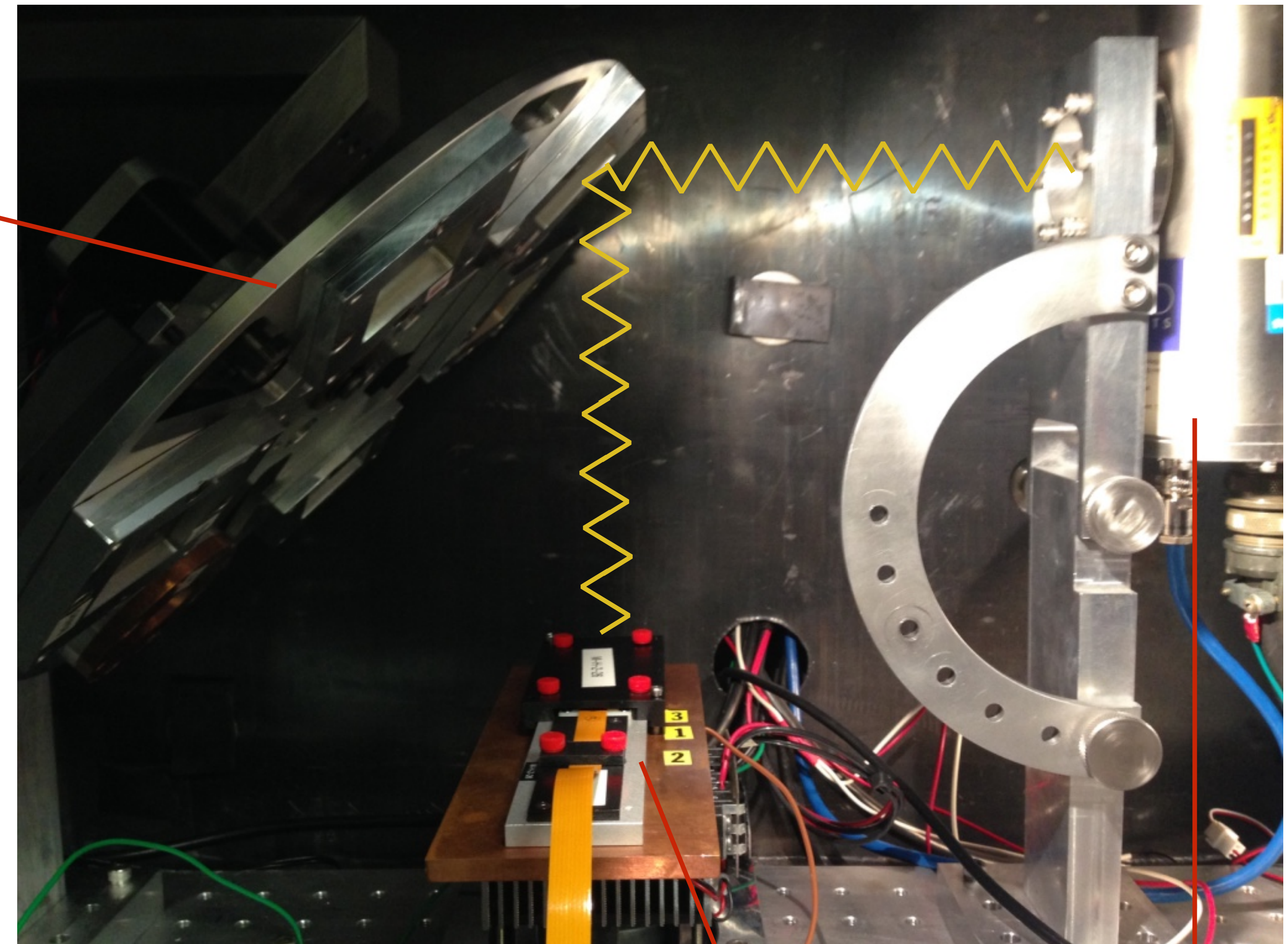
- Module calibration and (bulk of) qualification performed at FNAL
- Two test stands
  - Test 4 modules in parallel at each stand (~2 hours to calibrate and qualify at a single temperature)
- Tested 8 modules / day (average)





UIC X-Ray Test Stand

rotating stage



x-ray tube

module

x-ray tube power supply

interlock

reverse-bias power supply

FPIX Calibration and Qualification

Qualification

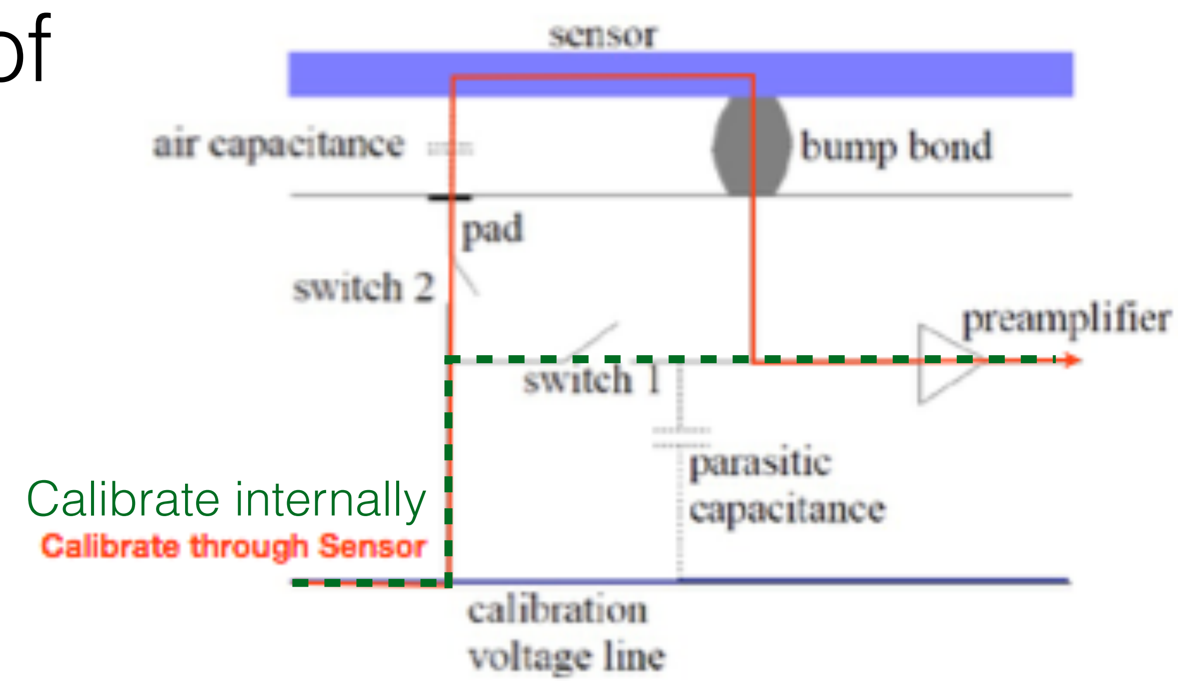
- Separate grades based on:
  - IV scan
  - Number of defective pixels (per ROC)
    - Dead, threshold defect, bad/missing bump
  - Number of defective double columns (per ROC)
    - Inefficient or prone to freezing
- Module grade is taken as the worst grade above

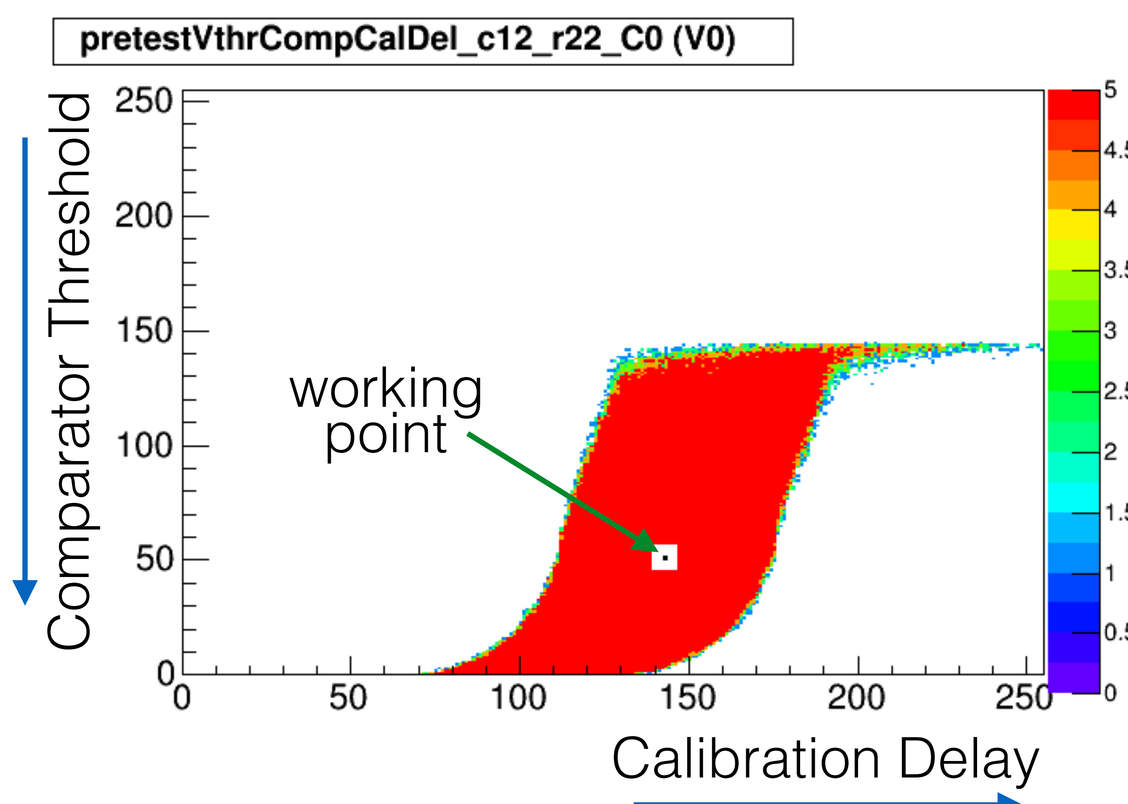
For example:

IV:	A	
defective pixels:	15 A, 1 B	$\rightarrow$ B
defective double columns:	16 A	

Pretest

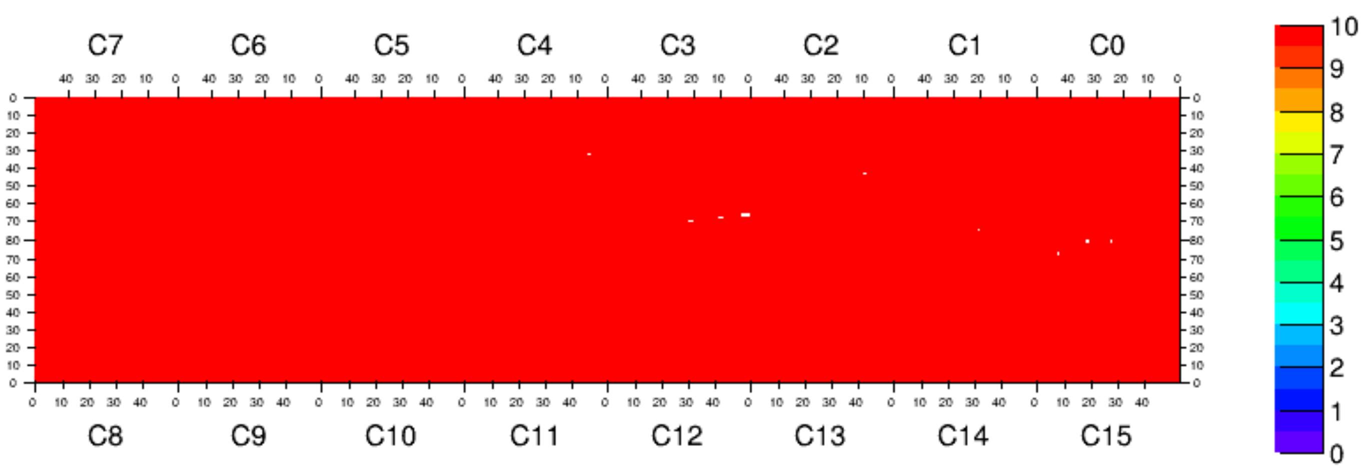
- Establish the basic functionality of the module and put it in an operational state
  - Test ROC programability
  - Tune analog current to nominal value
  - Test TBM timing parameters
  - Set the comparator threshold and calibration signal delay for each ROC

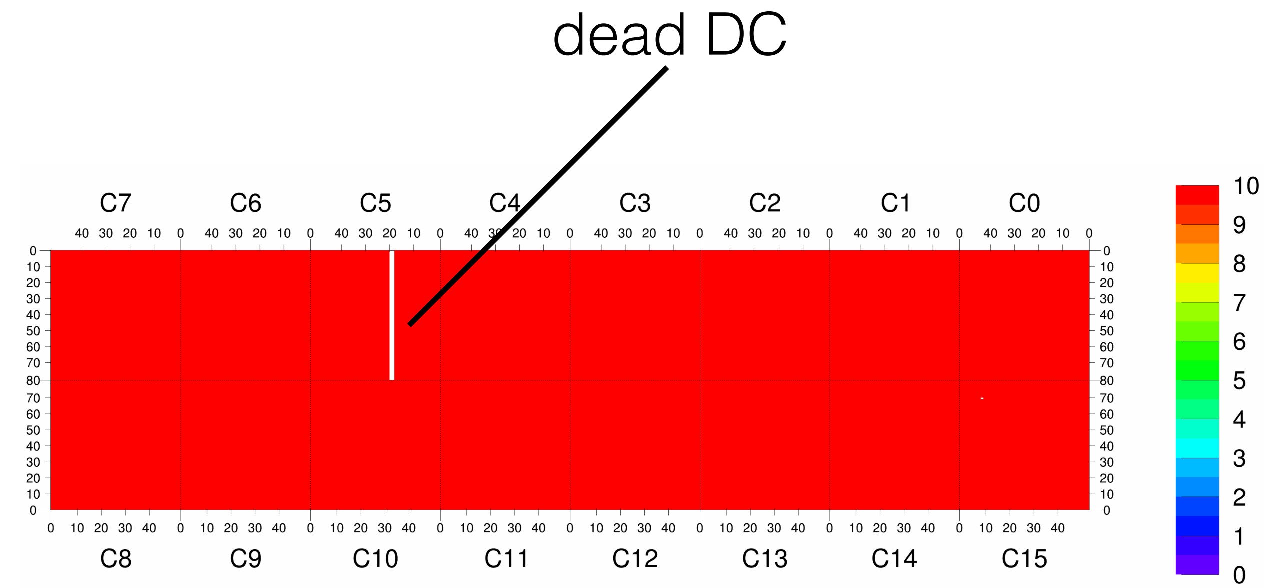




Pixel Alive Test

- Three-fold test that measures the basic functionality of the pixel unit cell
  - Inject calibration charge 10 times
    - Require 10 hits
    - Ensure correct addresses are reported
    - Ensure pixels can be masked
  - Pixels that fail any of the above are considered defective





Trimming

- Seeks to unify the response of all pixels
  - 1 ROC-wide DAC controls nominal comparator threshold
  - 4 trim bits **per pixel** (reduce effective threshold)
  - 1 ROC-wide DAC controls overall scale of trim bit effect (V_{trim})
- After trimming, all pixels should turn on at target signal (~1750 e^-)
- Trimming procedure:
  - Find pixel with largest amplifier gain
    - Disable all trim bits, set nominal comparator threshold to largest value such that this pixel fires when target calibration charge is injected
      - All other pixels will turn on above the target
  - Find pixel with smallest amplifier gain
    - Enable all trim bits, set V_{trim} to smallest value such that this pixel fires when target calibration charge is injected
      - All other pixels will turn on somewhere between the nominal threshold and this maximally-trimmed (minimum) threshold
  - For each pixel, perform binary search to determine trim bits such that pixel just turns on at target calibration charge

Trimming

- Seeks to unify the response of all pixels
  - 1 ROC-wide DAC controls nominal comparator threshold
  - 4 trim bits **per pixel** (reduce effective threshold)
  - 1 ROC-wide DAC controls overall scale of trim bit effect (V_{trim})
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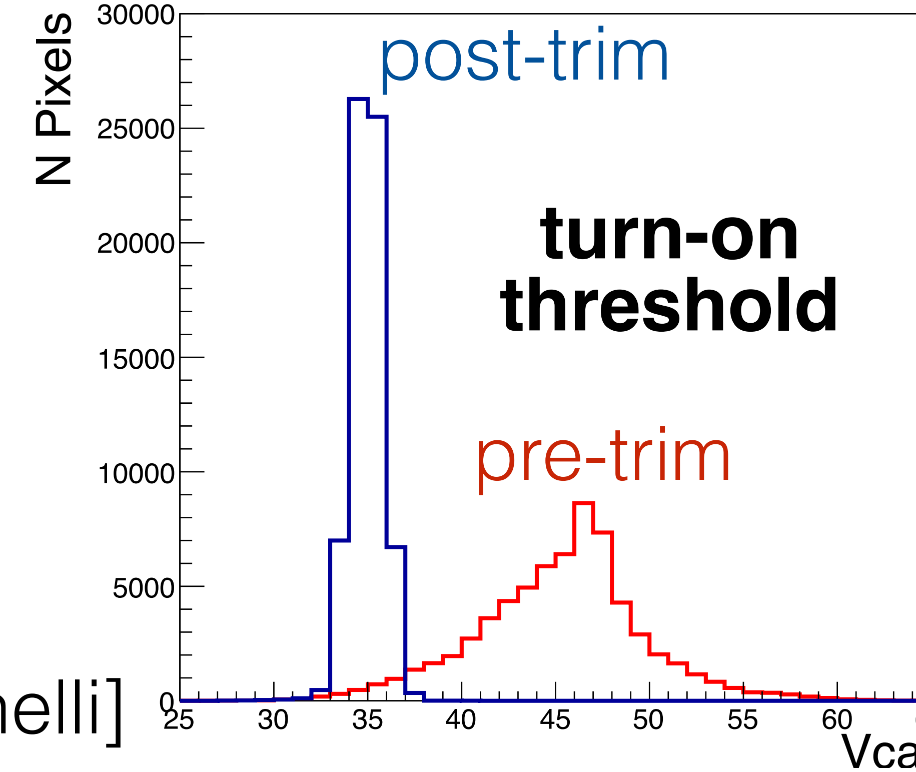
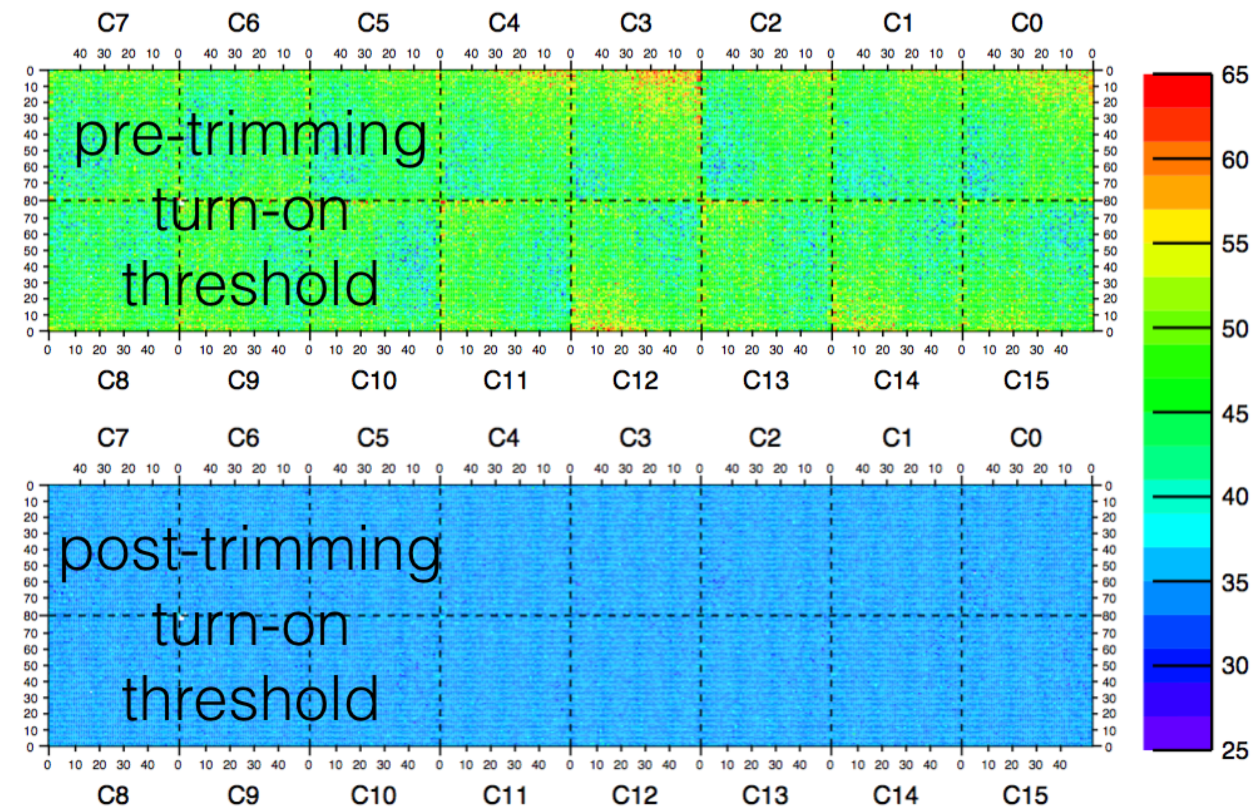


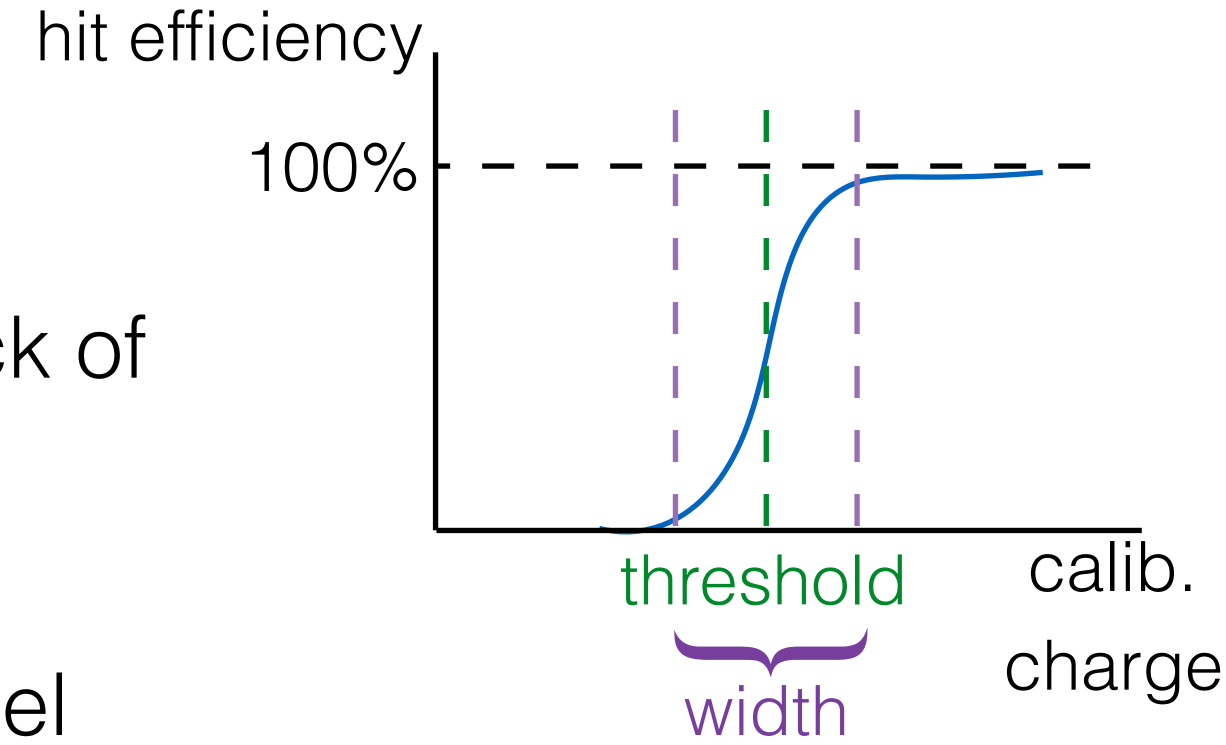
[Jamie Antonelli]

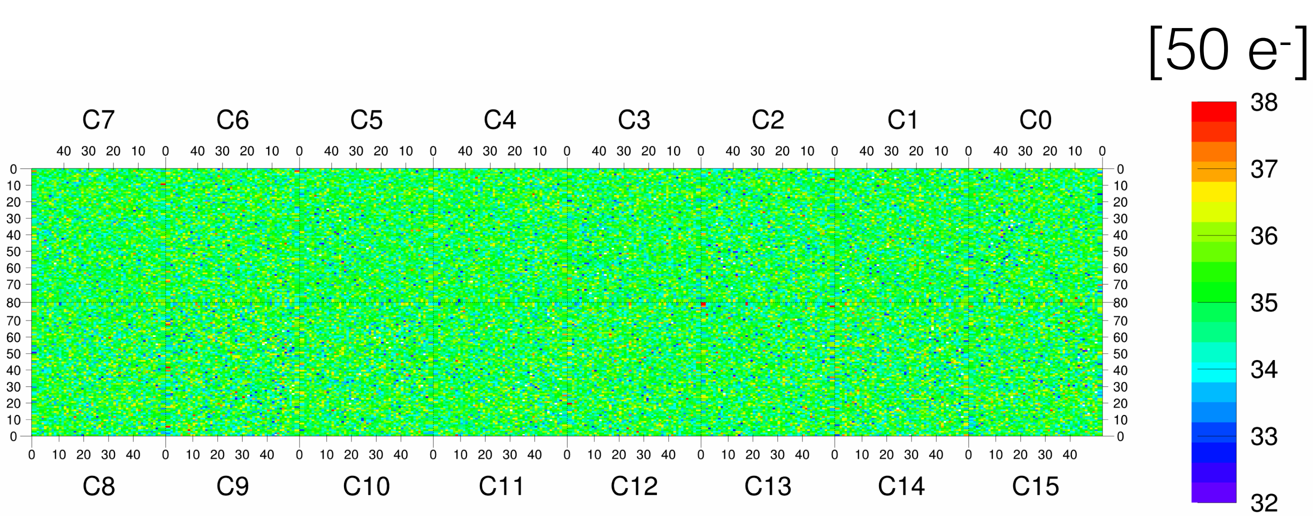
Pixels which can't be trimmed to target threshold are considered defective

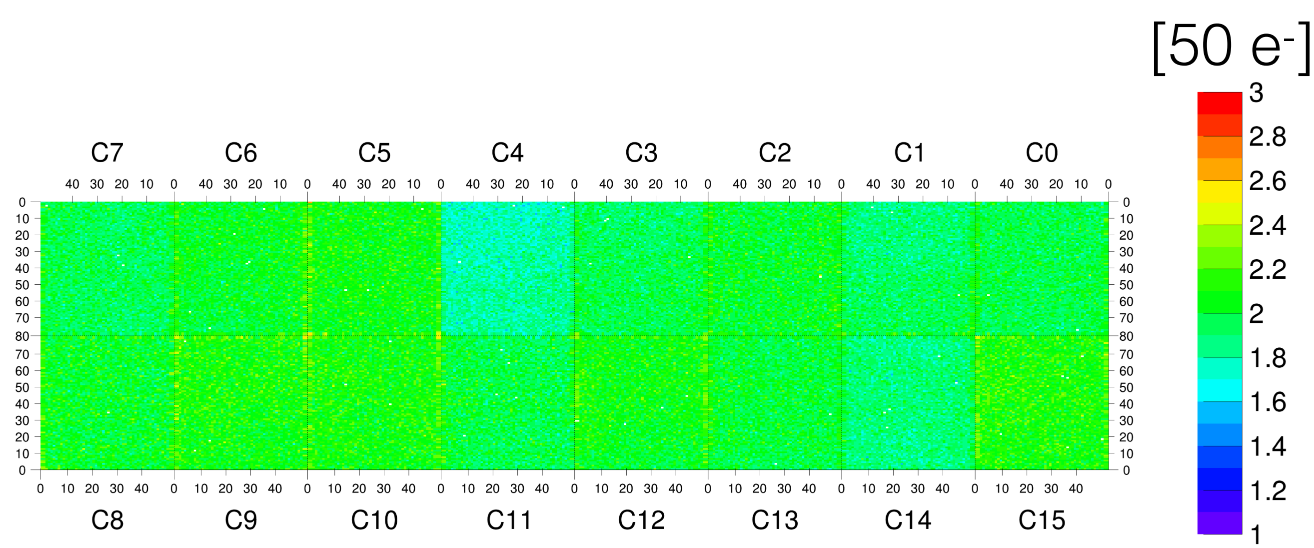


S-Curves

- Measure s-curves w.r.t. calibration charge
  - Turn-on threshold provides check of trimming
  - Turn-on width provides a measurement of the pixel-by-pixel noise
    - Typical values are ~100-150 e$^-$

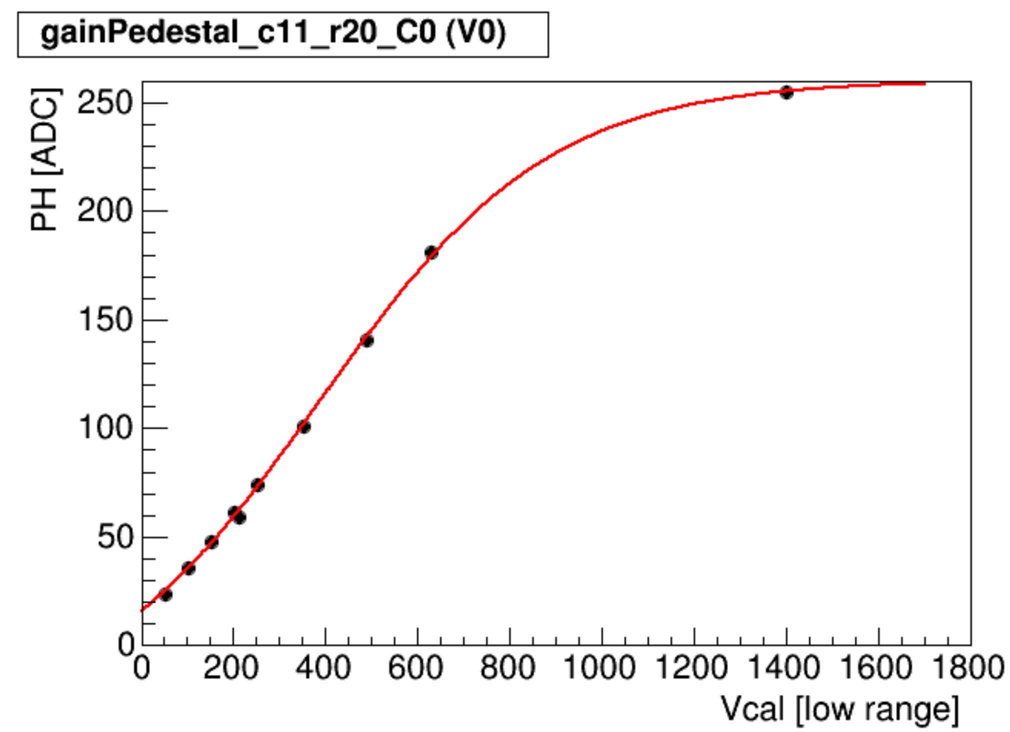


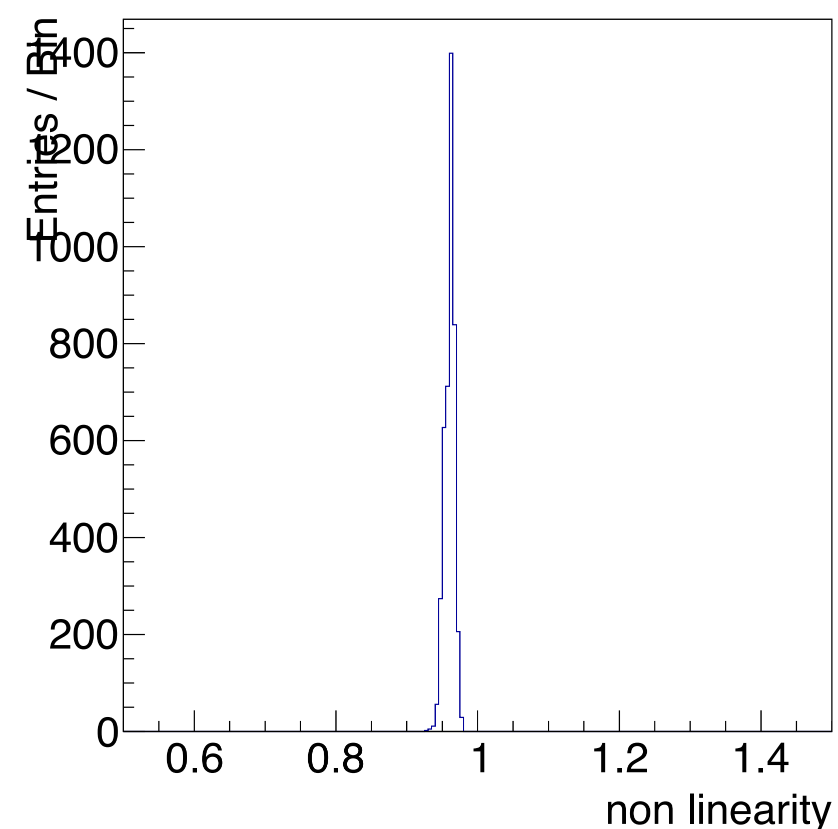




Pulse Height Optimization

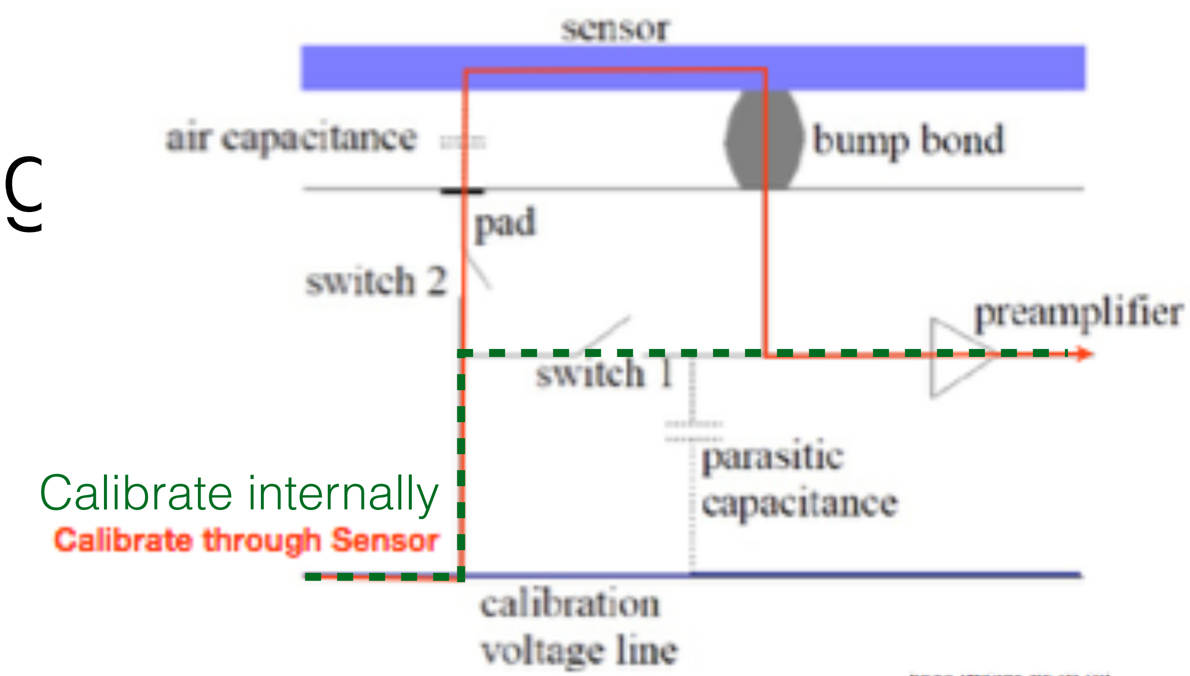
- Fit an error function to PH vs calibration charge
    - X-ray calibration (described later) allows conversion to signal charge
- True integral of error function compared to linear approximation to determine non-linearity

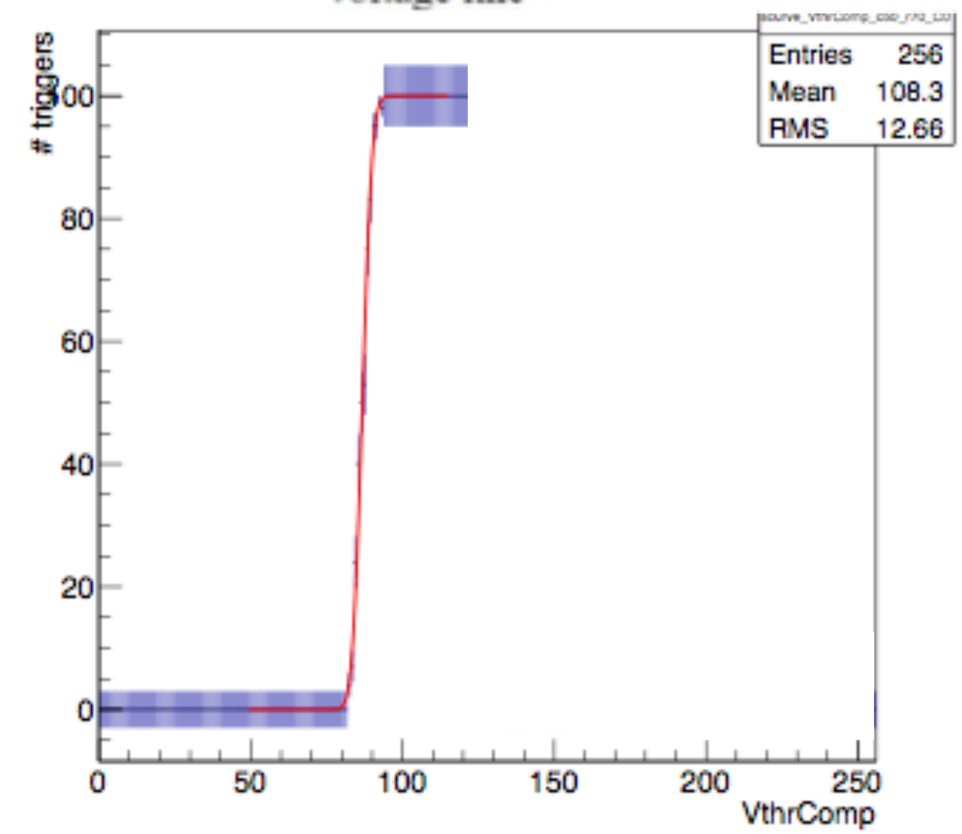




Bump Bonds

- Inject calibration charge into sensor via capacitive coupling
- Check comparator threshold at which pixel turns on
  - Bad/damaged bonds require a lower threshold in order to register hit
    - Pixels/bumps ≥5σ from mean are considered defective





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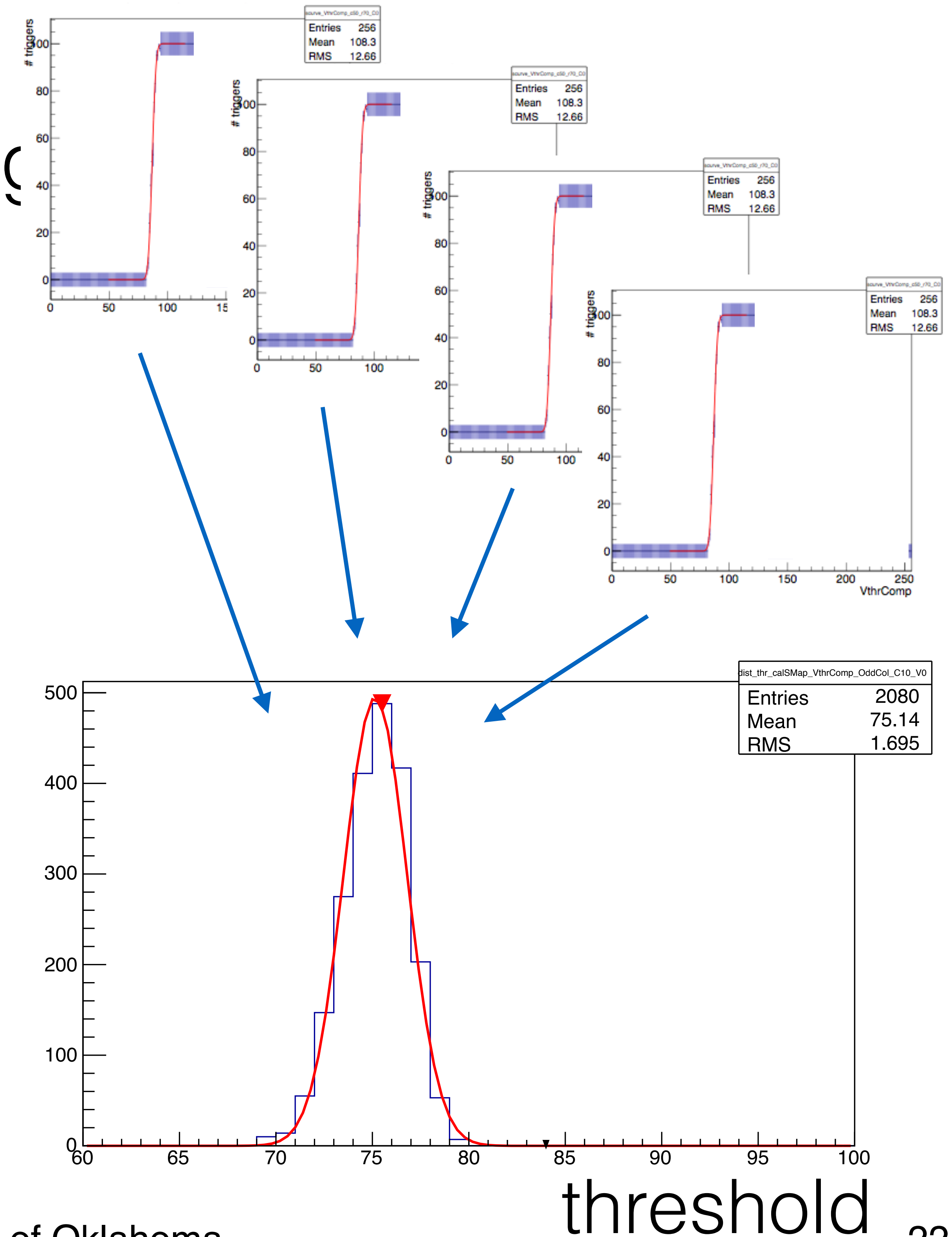
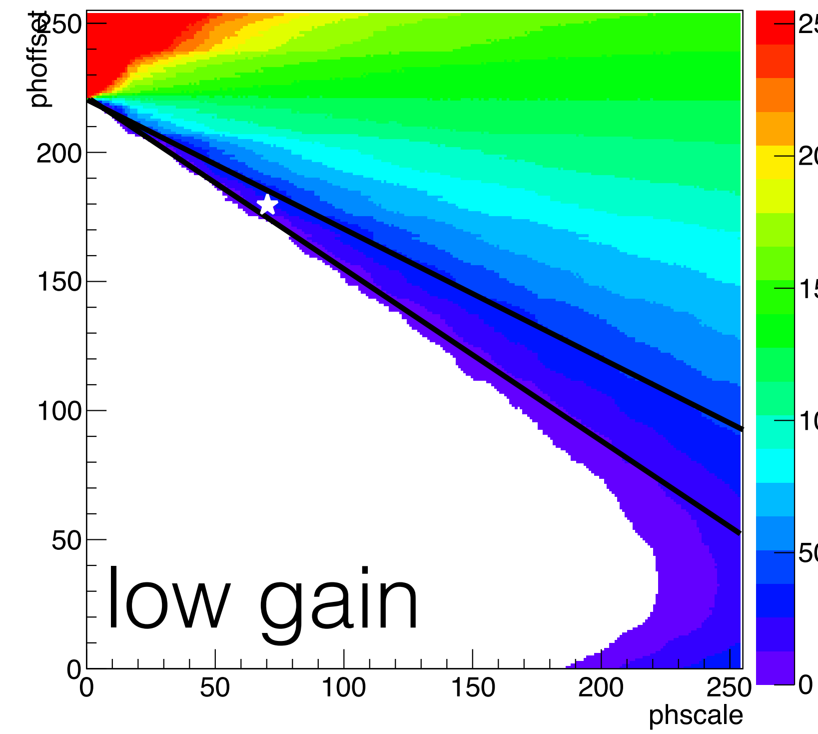
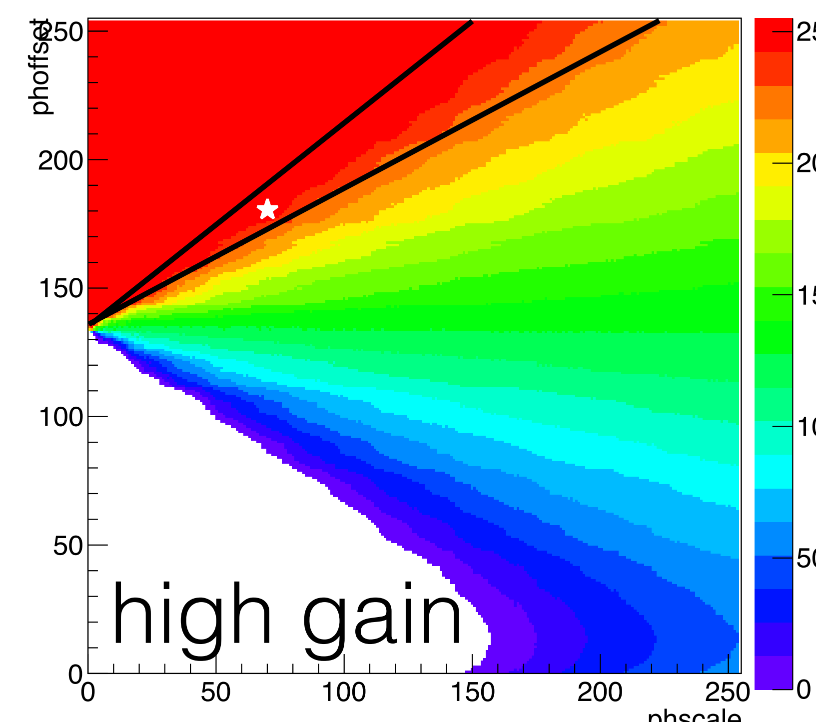


Pulse Height Optimization

- Optimize the dynamic range of the 8 bit ADC
  - Controlled by PHOffset and PHScale DACs
- Find pixels with high and low inherent gain
  - Low gain pixel PH should provide PH well above noise at turn-on
  - High gain pixel should saturate for large signal charge
- Each of the above criteria defines a band → choose working point from intersection of bands

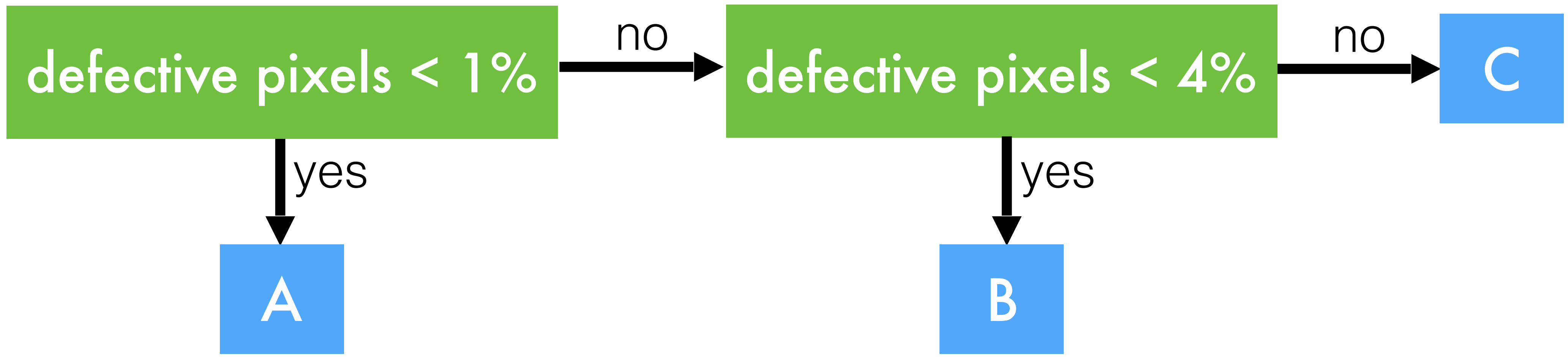
pulse height scans





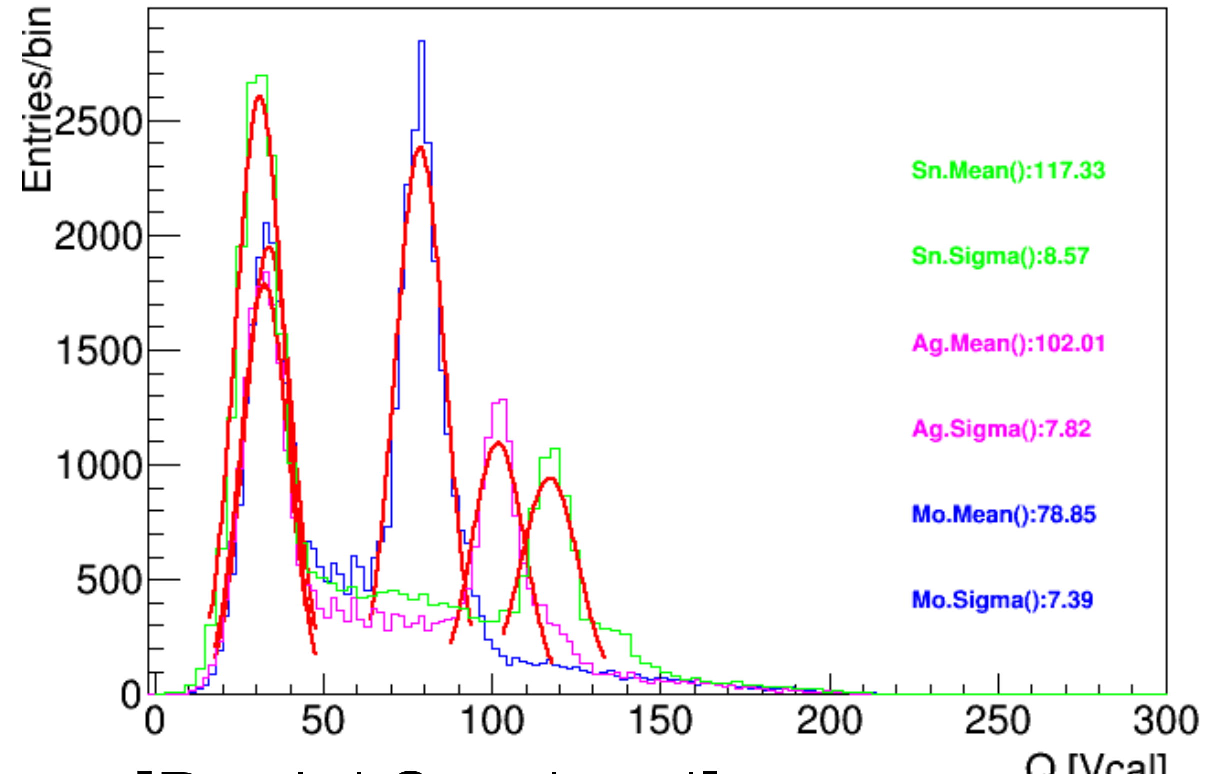
ROC Grading

- Defective pixel
  - Fails pixel alive test
  - Turn-on can’t be tuned properly
  - Bad/missing bump

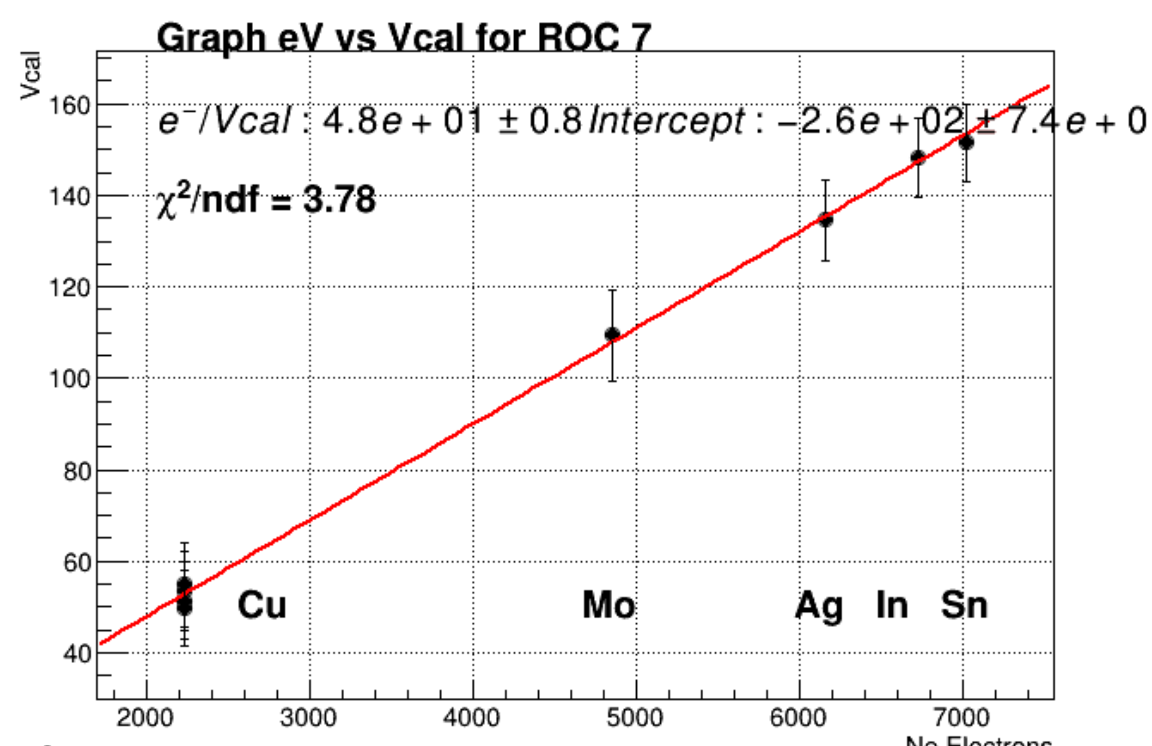


X-Ray Flourescence

- Provides absolute energy calibration
  - Use foils to obtain characteristic x-rays at various energies
- Performed on all early modules, but later only 1 module / wafer

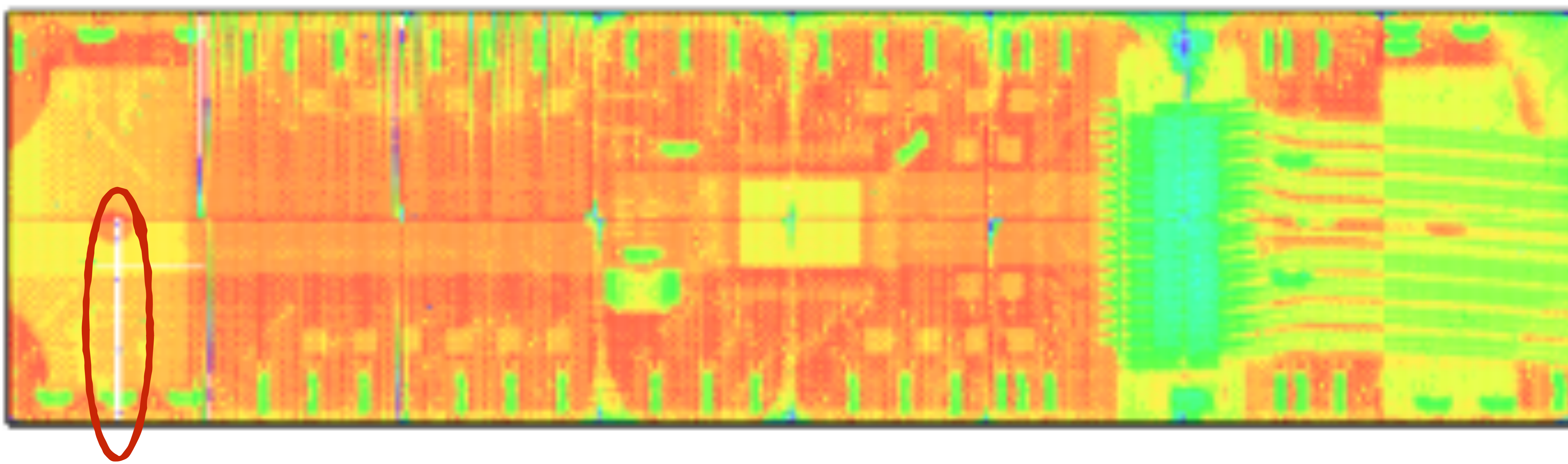


[Daniel Sandoval]



High-Rate X-Ray Test

- Rate of calibration charge injection limited to several bunch crossings
- High-rate x-ray test can identify problems in the periphery logic and in the readout buffers of the ROCs that are otherwise undetectable
  - Double column inefficiency or freezing



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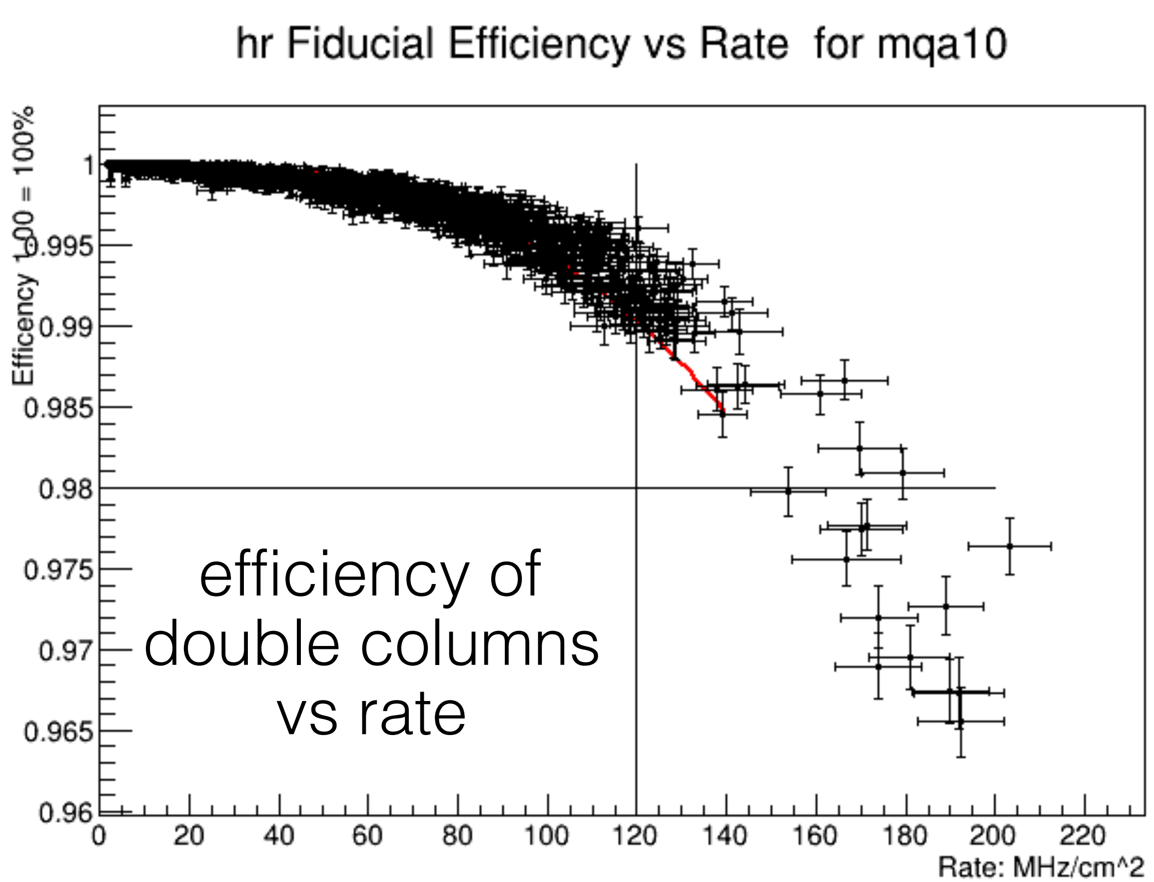
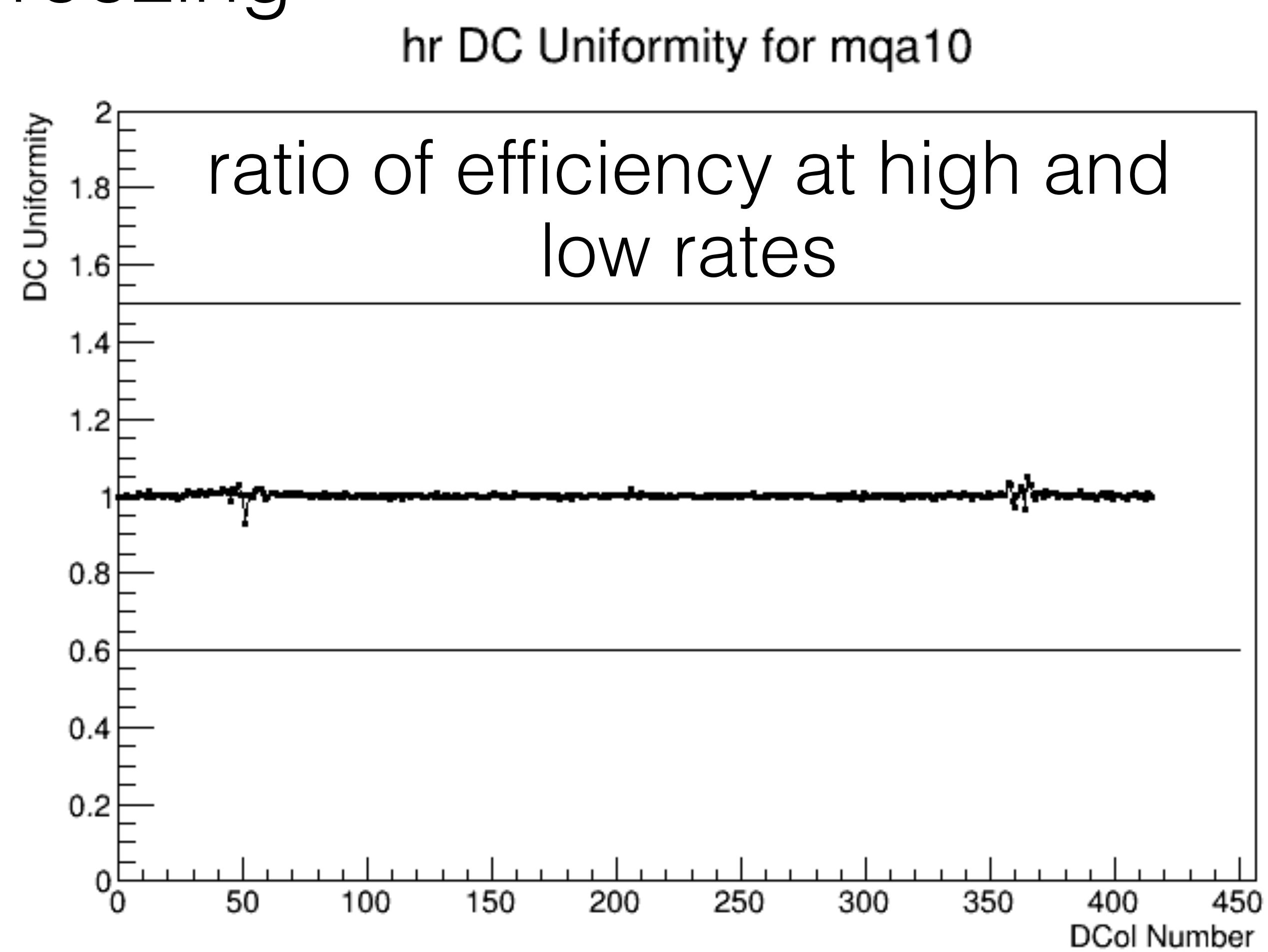
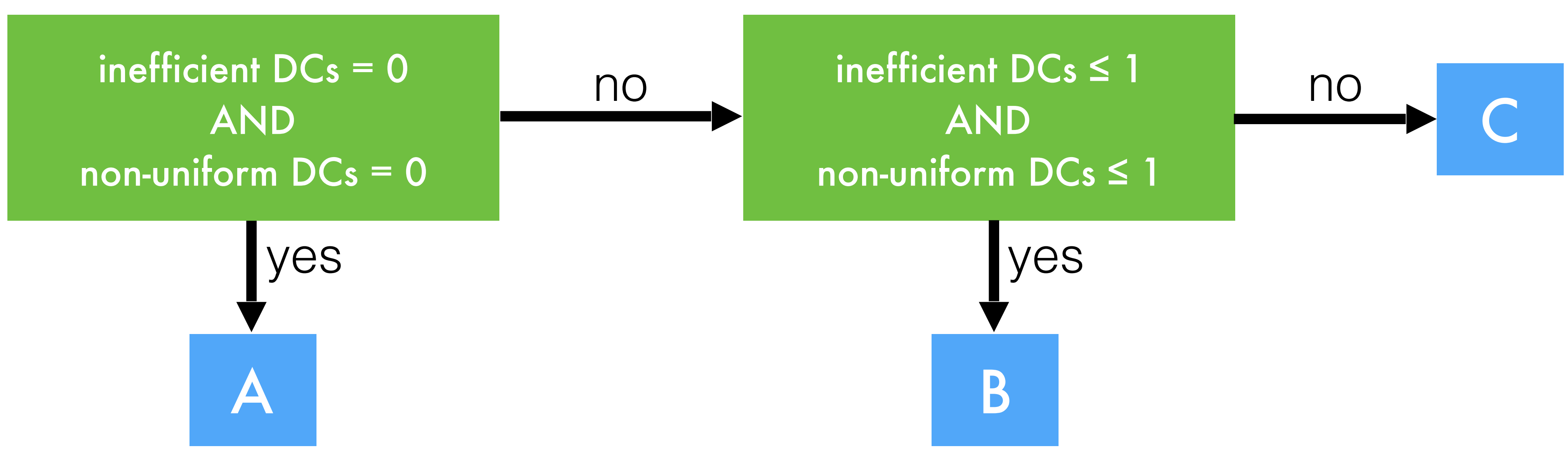




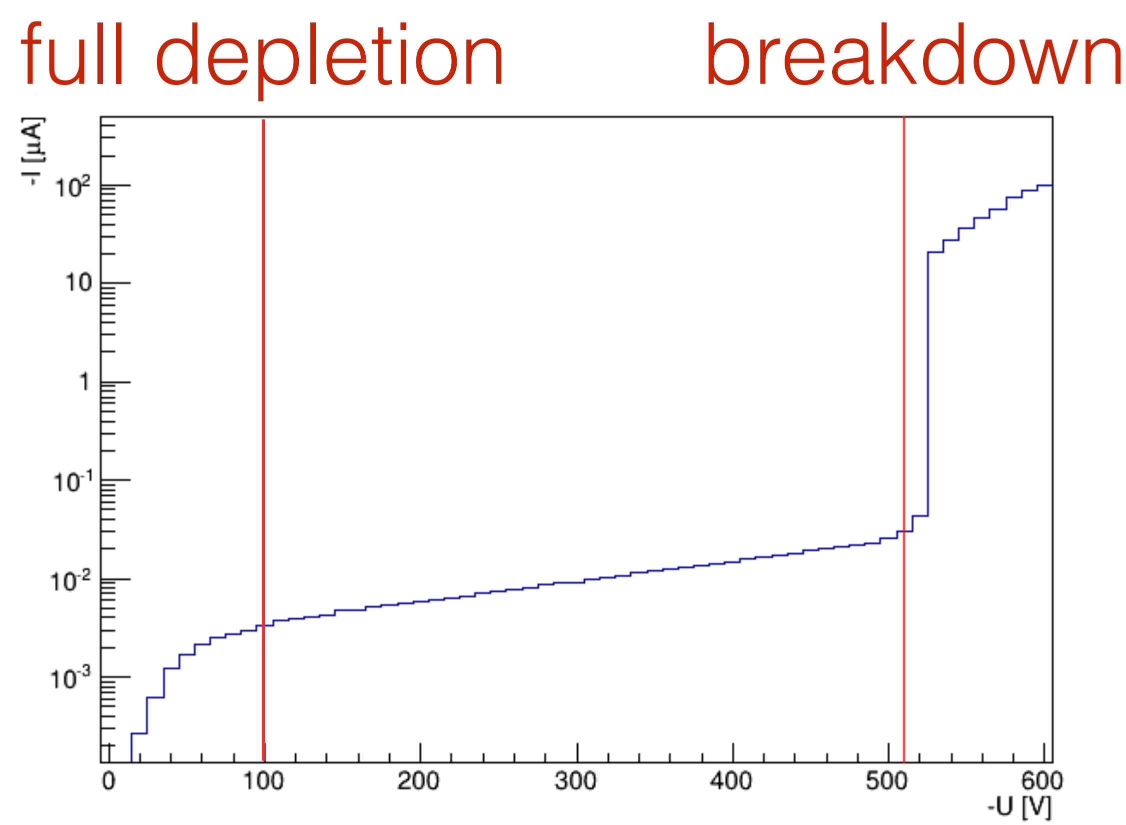
ROC X-Ray Grading

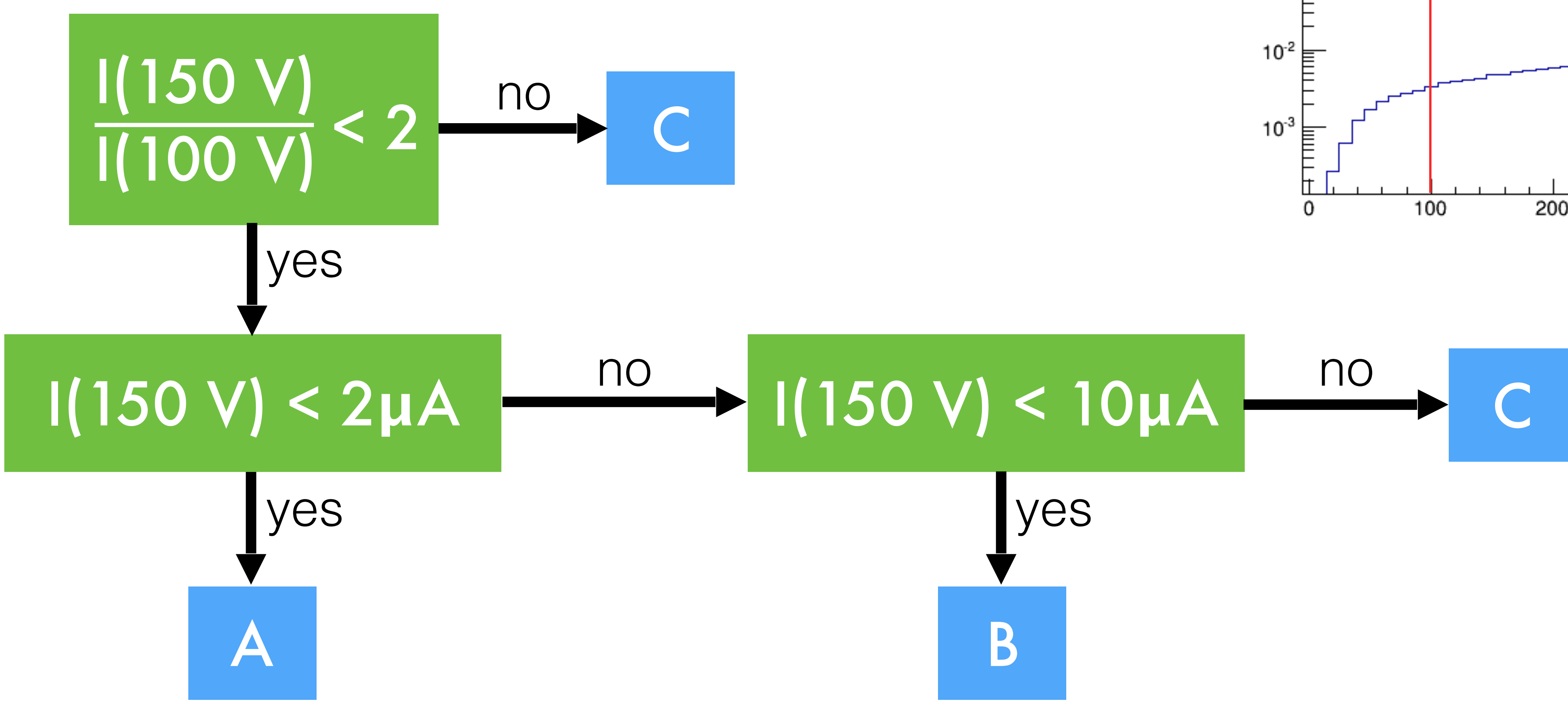
- Inefficient double column
  - High-rate efficiency < 98%
- Non-uniform double column
  - Ratio of high- and low-rate efficiencies < 0.6



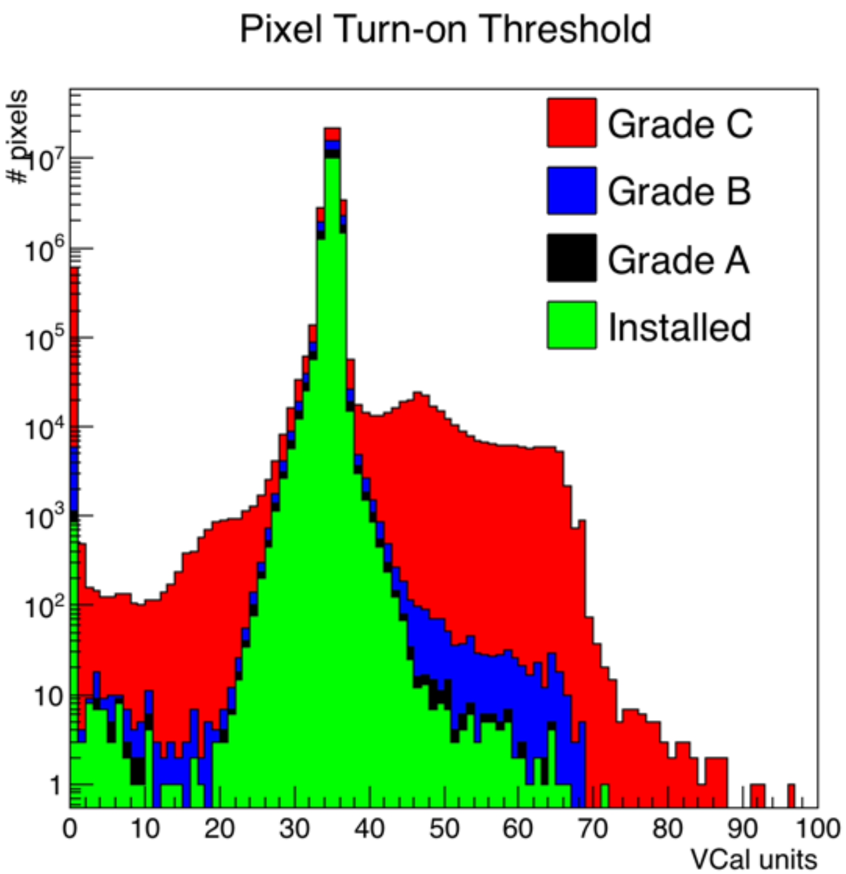
IV Grading

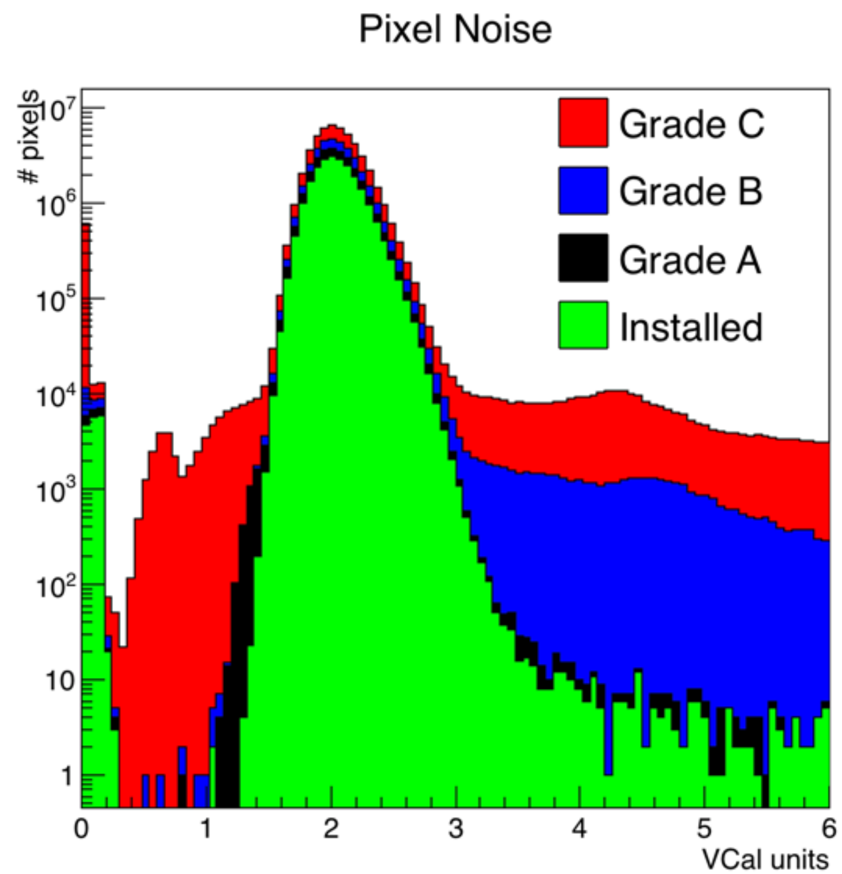
- Scan reverse-bias voltage and measure current draw

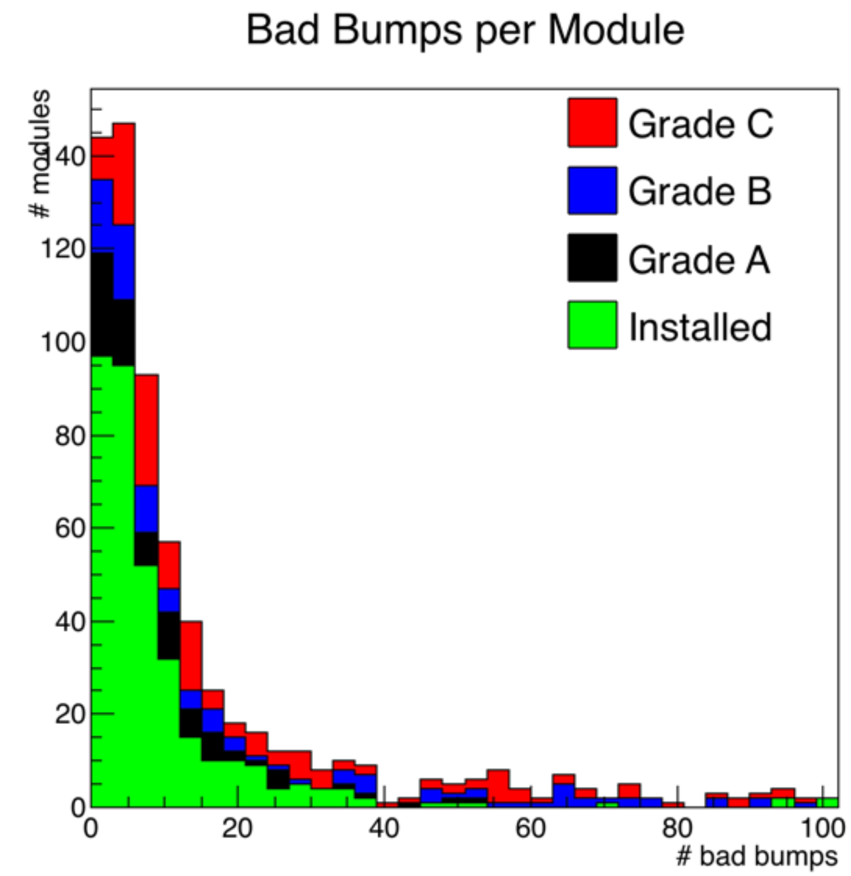


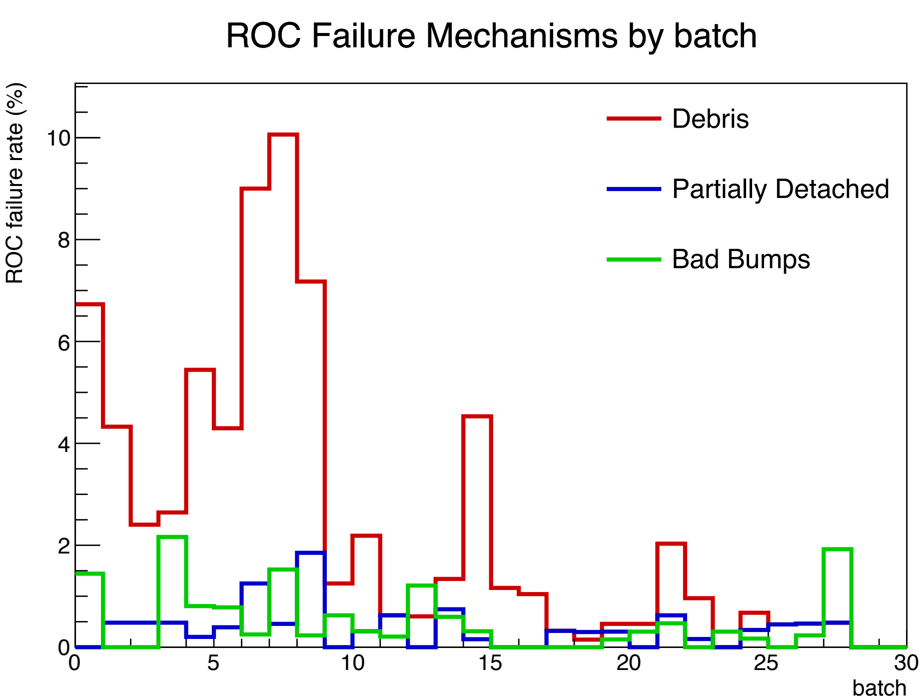


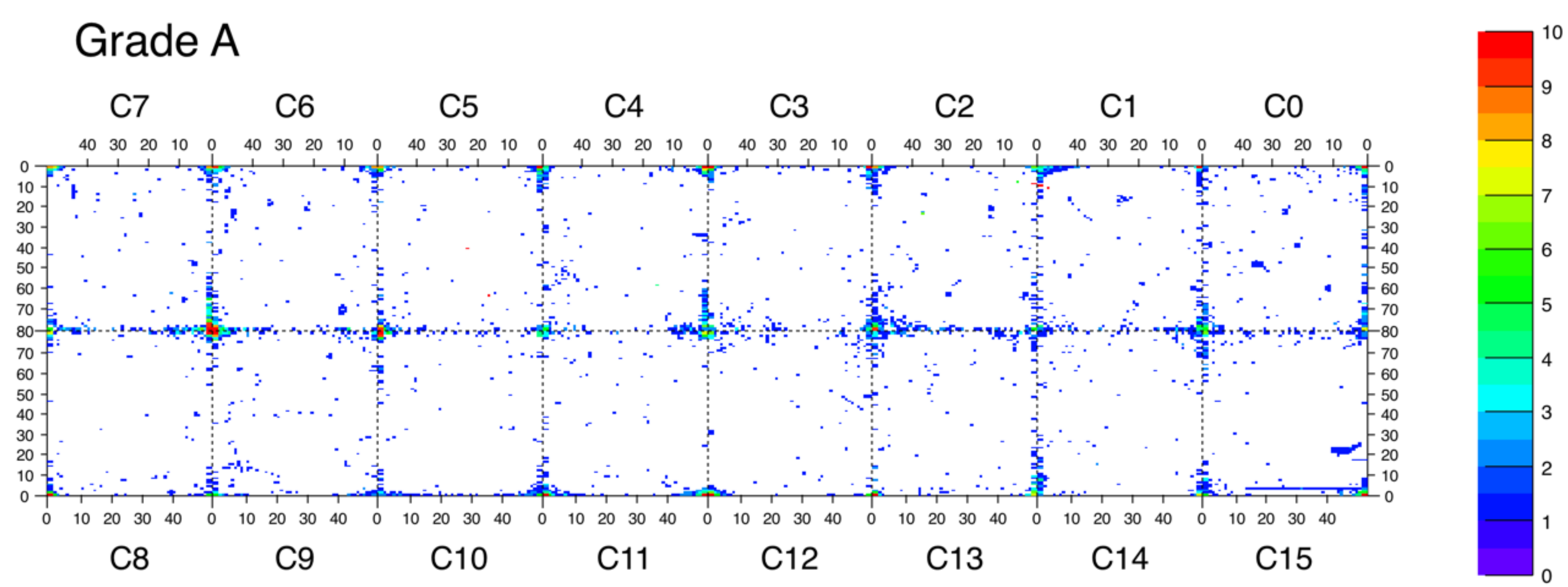
Module performance plots











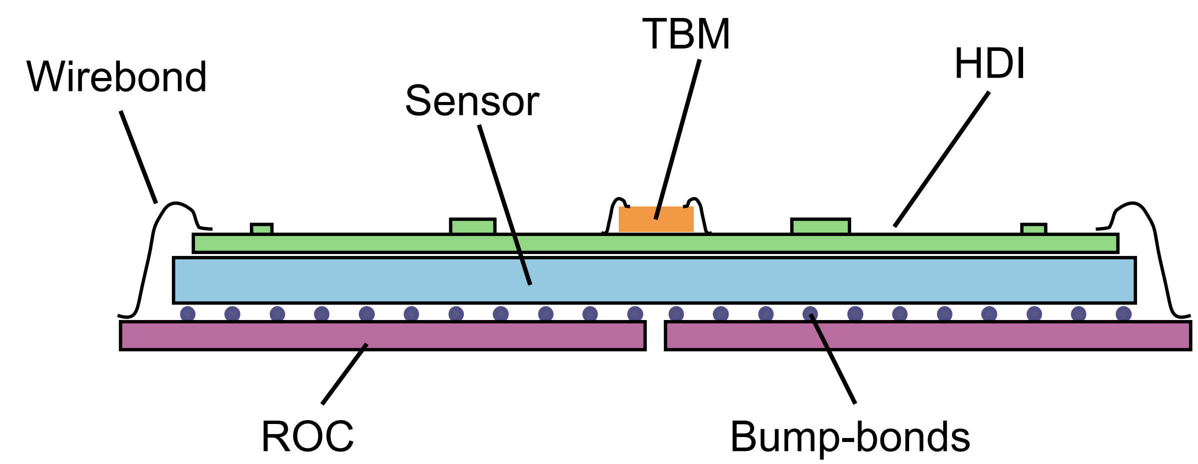
Conclusion

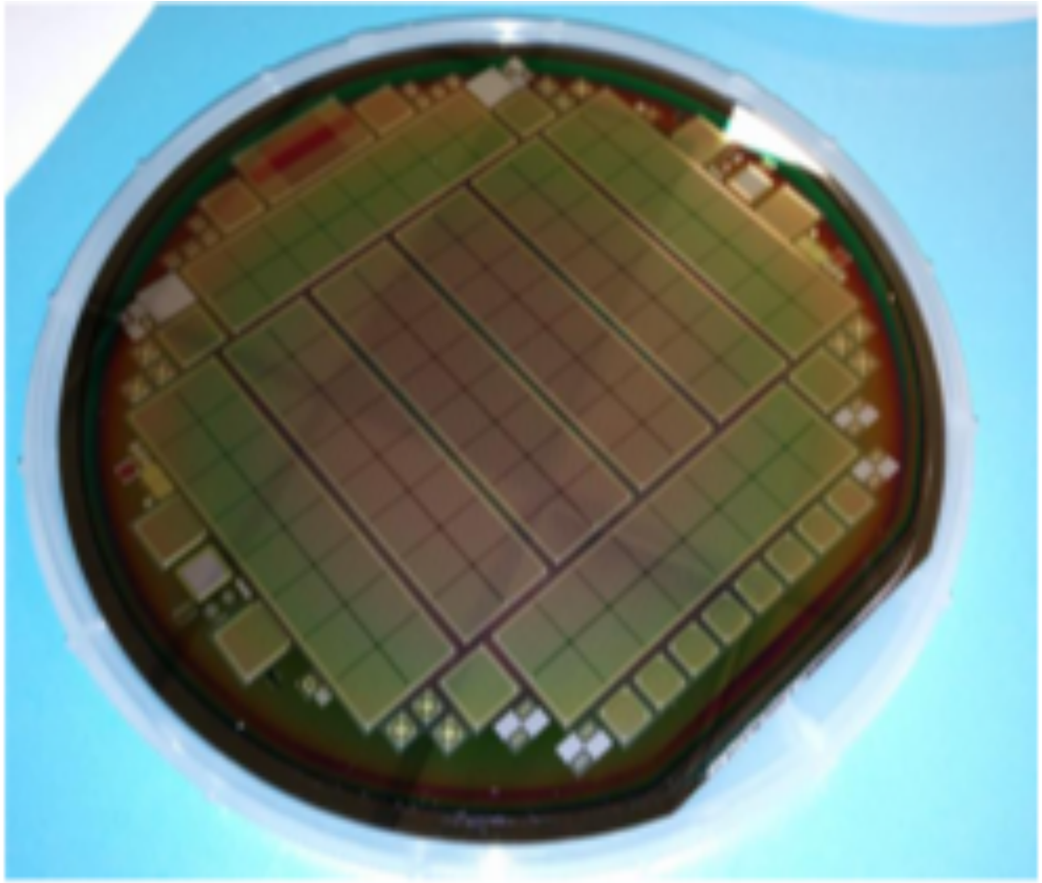
- Summary of CMS Phase I pixel module assembly, calibration, and qualification procedures
    - Hopefully some ideas can be borrowed to benefit the ATLAS Phase II upgrade

Backup

Module Components

- Sensor
  - Diced/probed by SINTEF
  - IV scan repeated upon delivery to FNAL
- PSI46dig readout chip (ROC)
  - Wafers tested at FNAL, then diced by RTI
- High-density interconnect (HDI)
  - Production + Initial testing by Compunetics
  - Visual inspection, electrical tests, and installation of surface components at FNAL
- Token bit manager (TBM08c)
  - Tasted on the wafer, then diced





Qualification Workflow

Assembly Testing

@17C

- IV
- Pretest
- ≥5 thermal cycles (-30C to 50C)
- IV
- Pretest
- Pixel alive
- Trim
- Bump bonding

Calibration Testing

@17C

- IV
- Pretest
- Pixel alive
- Trim
- Pulse height optimization
- Gain pedestal
- Bump bonding
- S-curves

~10%

~90%

X-Ray Testing

@17C

- Fluorescence Test
- High Rate Test

@-20C

- IV
- Pretest
- Pixel alive
- Trim
- Pulse height optimization
- Gain pedestal
- Bump bonding
- S-curves

Purdue/Nebraska

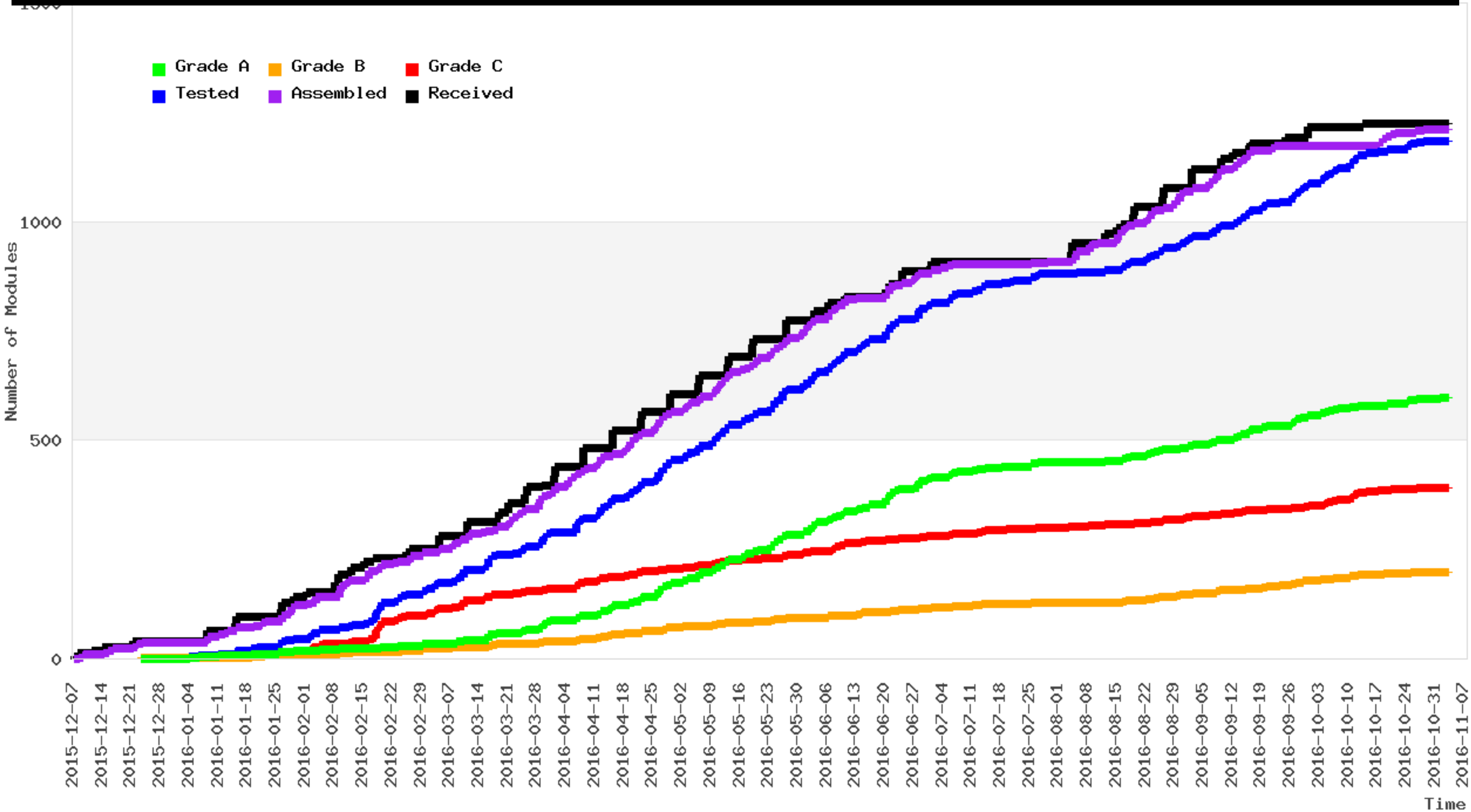
FNAL

University of Illinois - Chicago/Kansas

Trimming

- Seek to unify the response of all pixels
  - 1 ROC-wide DAC controls nominal comparator threshold
  - 4 trim bits **per pixel**
  - 1 ROC-wide DAC controls overall scale of trim bit effect (V_{trim})
- After trimming, all pixels should turn on at ~1750 e^-
- Trimming procedure:
  - With trim bits disabled, set injected calibration charge to 1750 e^- and measure s-curves w.r.t. comparator threshold
    - Ignoring 2σ outliers, set comparator threshold to largest value for which any pixel registers a hit (all pixels turn on at or above target calibration charge)
  - With all trim bits enabled (reduced comparator threshold), measure s-curves w.r.t. injected calibration charge
    - Set V_{trim} to smallest value such that all pixels fire
  - Perform binary search to set trim bits for each pixel

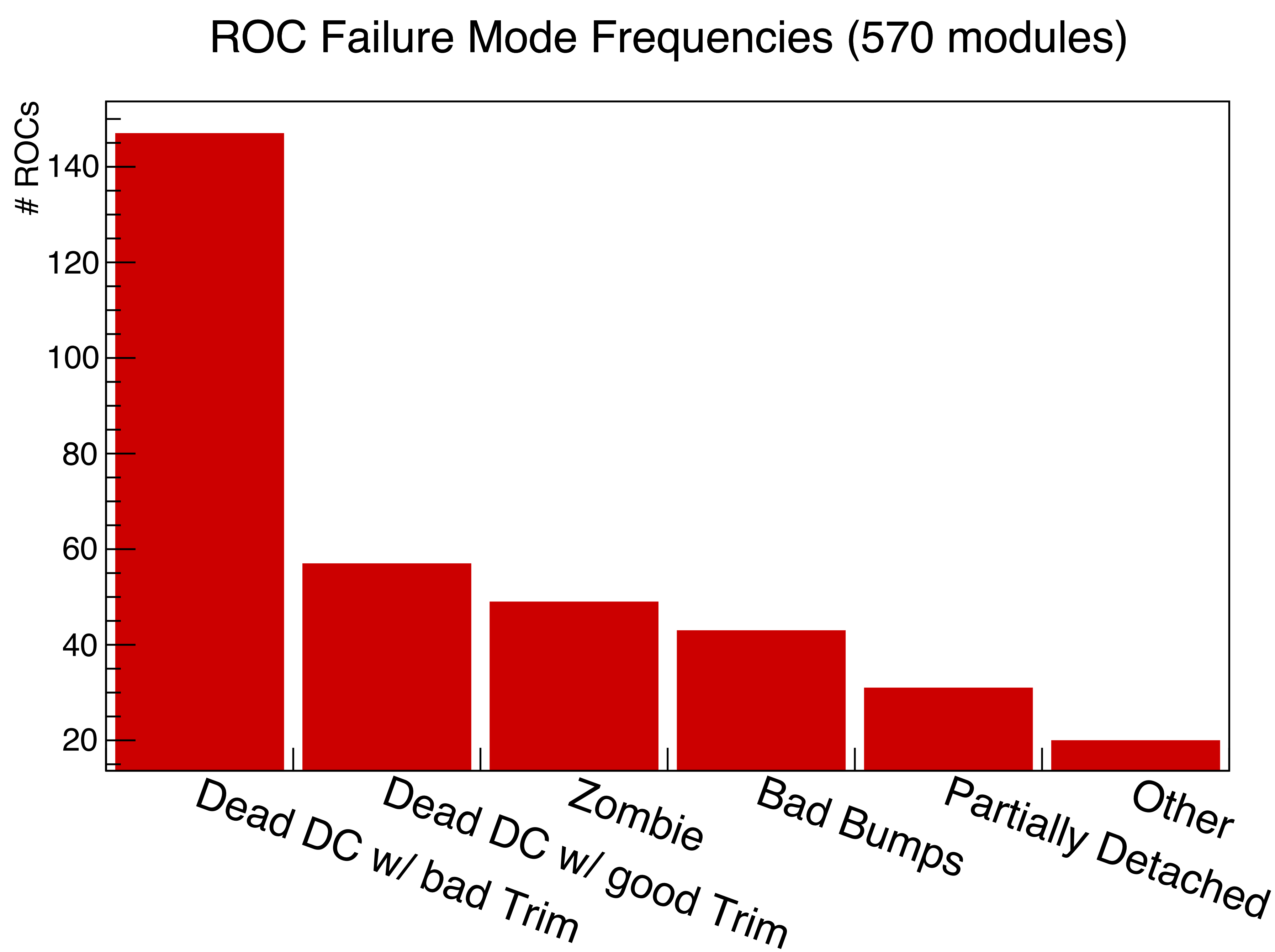
Production Summary



Production failure mode breakdown

TBM failures (replace TBM and retest)
Sensor failures (IV: very few failures)
ROC failures dominate (see plot)

The following slides will detail the various ROC failure modes and their causes



Failure Mode: Dead double columns & zombie ROCs

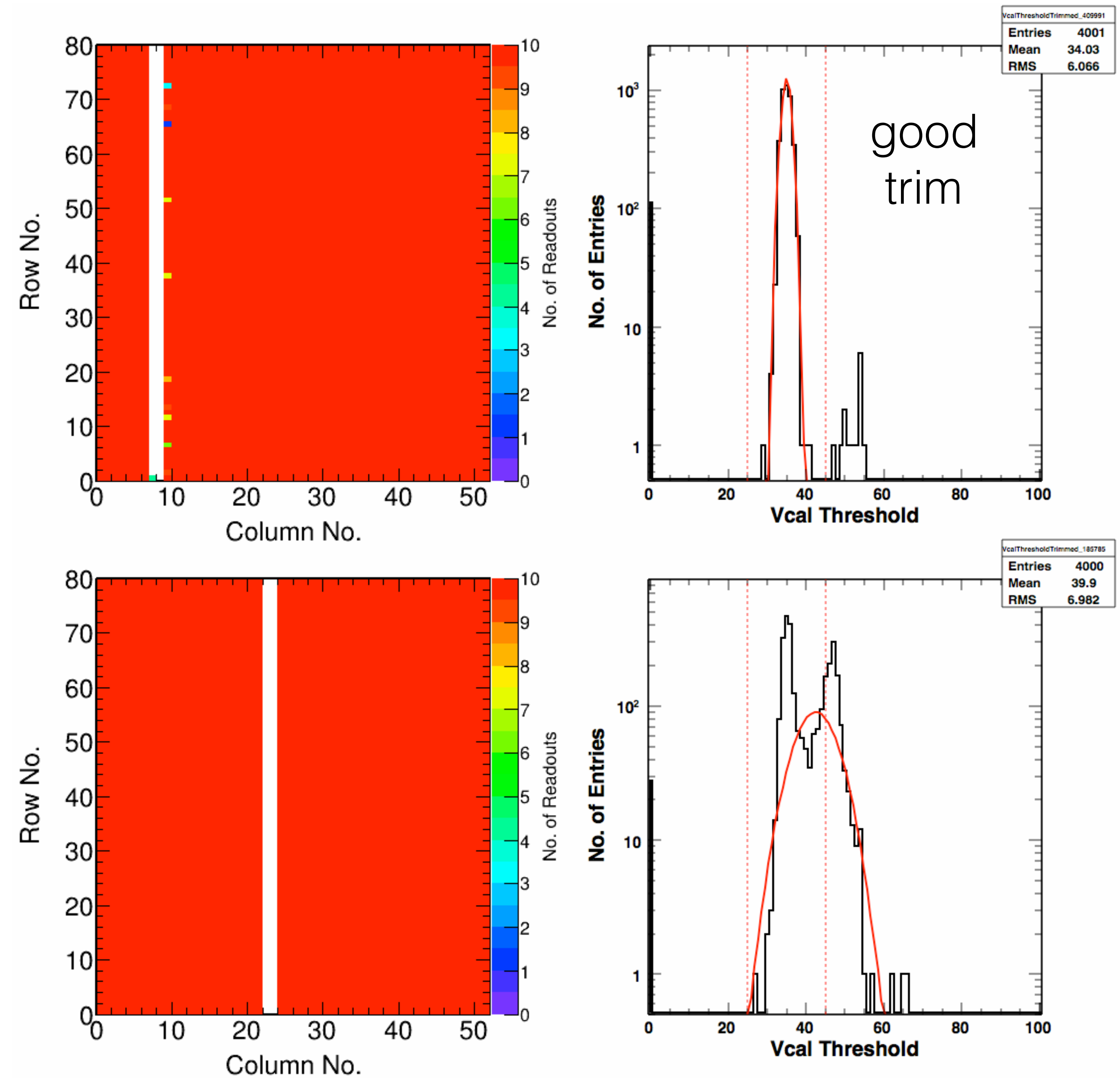
Dominant failure modes so far in production

Readout is done via a double column drain mechanism, so this means one readout circuit is dead

Dead DC can draw more current so that rest of ROC is underpowered

In this case, often pixels can't fire at the low thresholds required for trimming

"Zombie" ROCs give no data but don't affect module data stream



Cause: Dicing debris

Once bump bonds are deposited on ROC wafers, the wafers are diced into individual ROCs with a saw

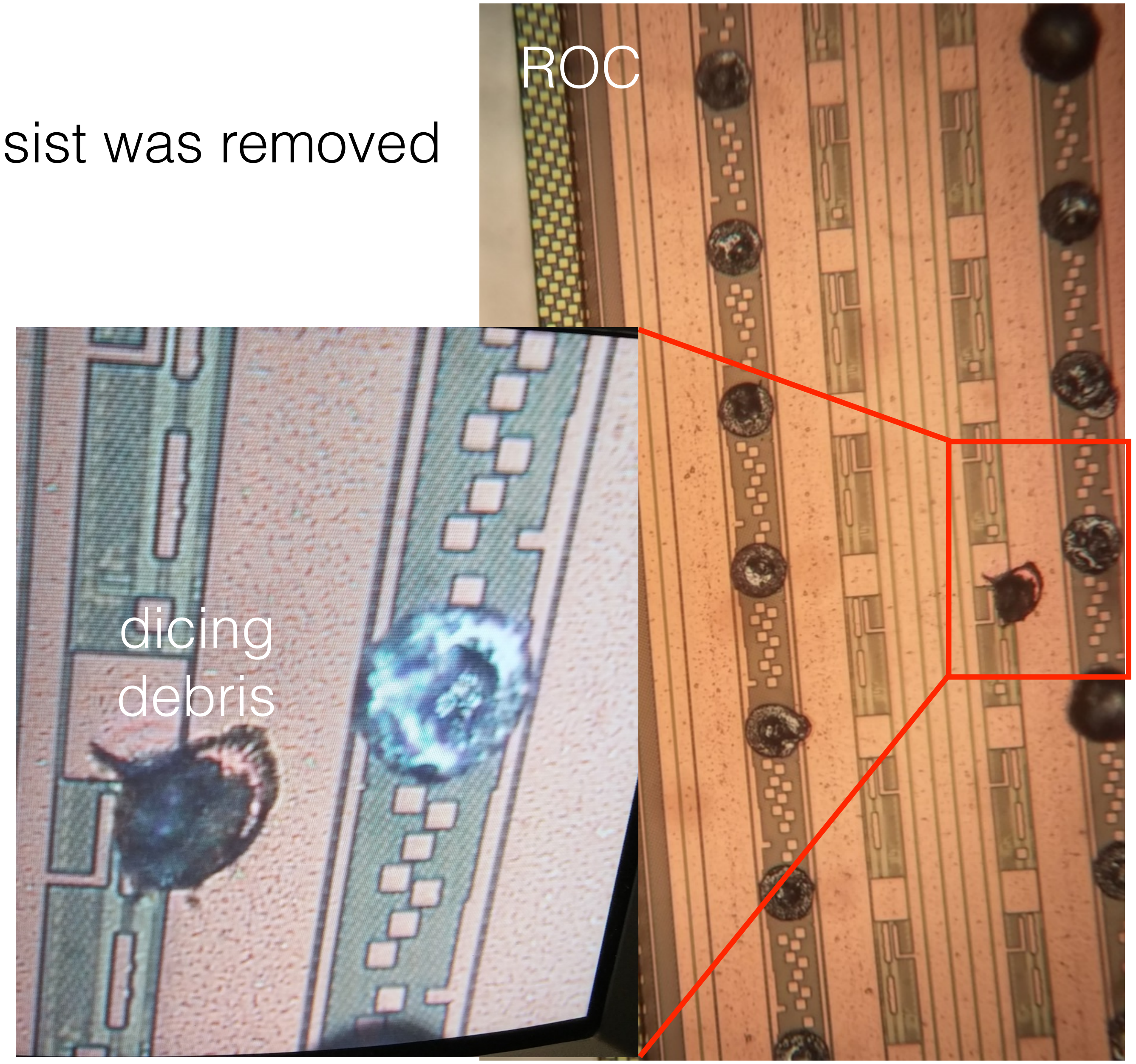
During pre-production, a layer of photoresist was still present on the ROC surface during dicing, being removed later

To save time during production, the photoresist was removed before wafer dicing

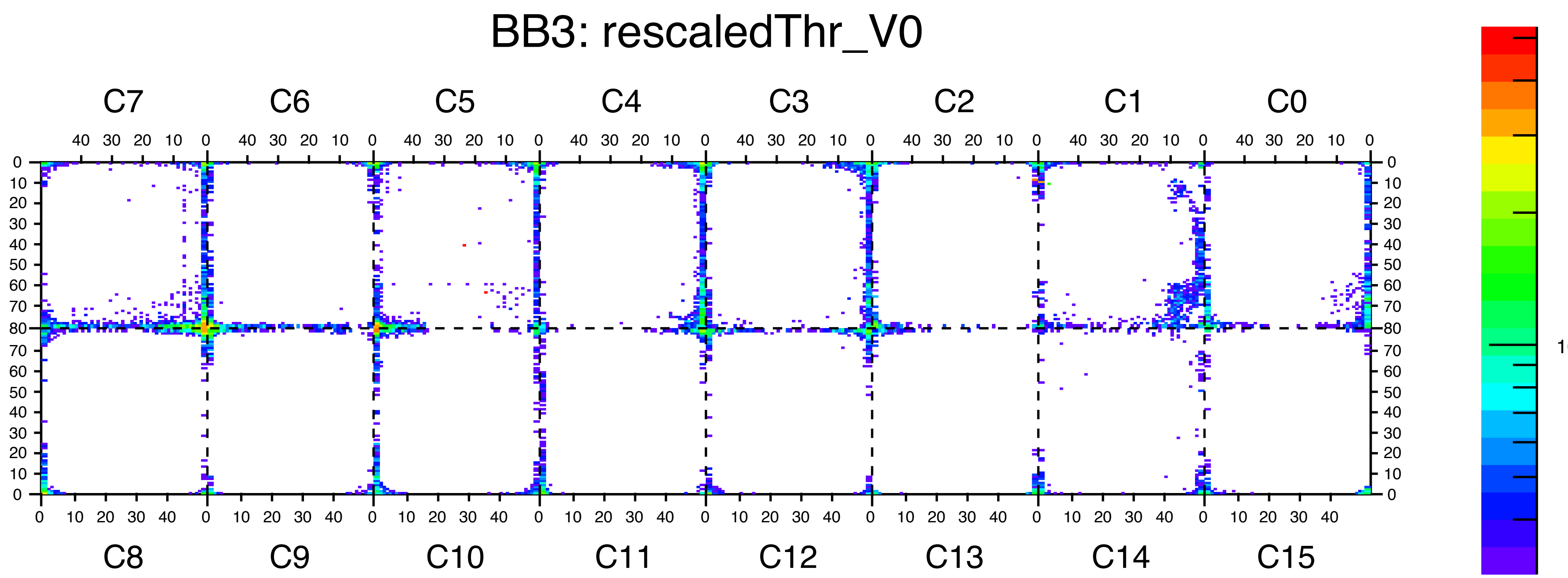
This often caused silicon debris from the dicing saw to get lodged on the ROC surface

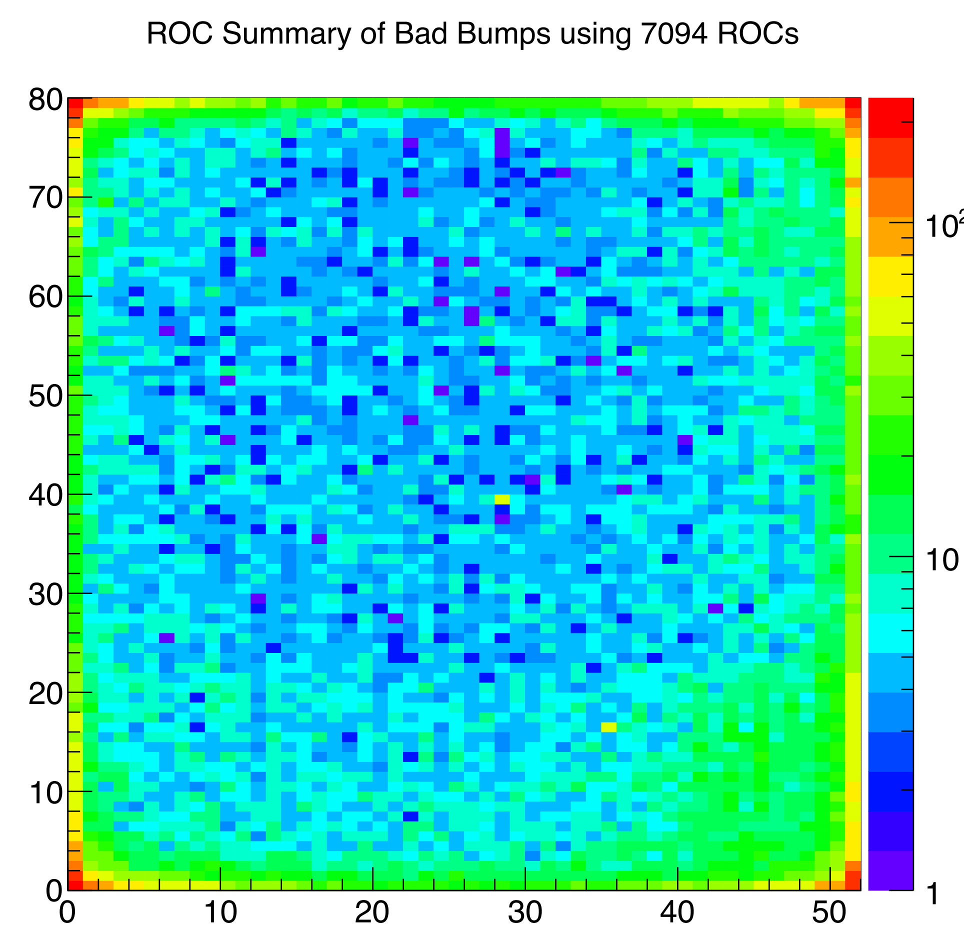
If debris is present in the active area of the ROC, it causes a double column failure

If debris is present in the periphery, the entire ROC can be affected



Failure Mode: Damaged bump bonds



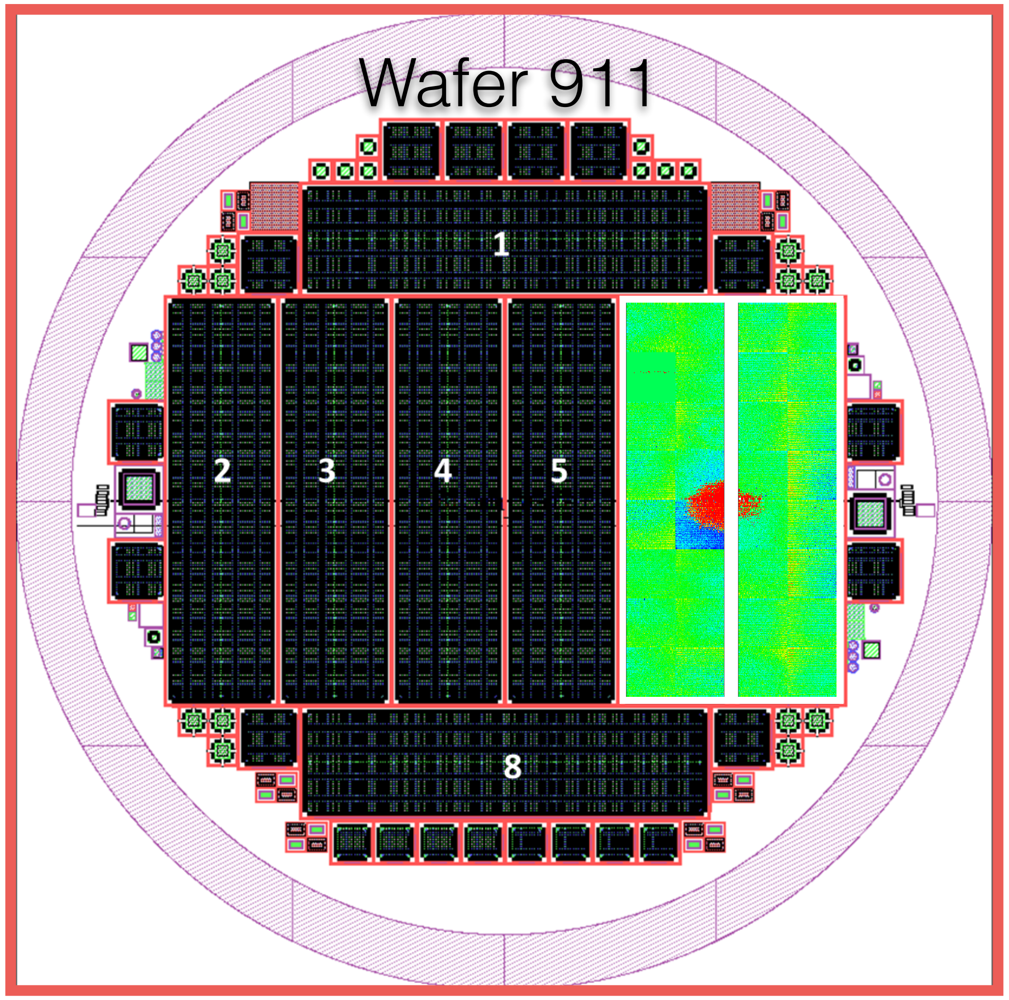


plots show the sum of bad bumps in otherwise good ROCs for ~450 modules

~0.1% of bump bonds are damaged during production/testing

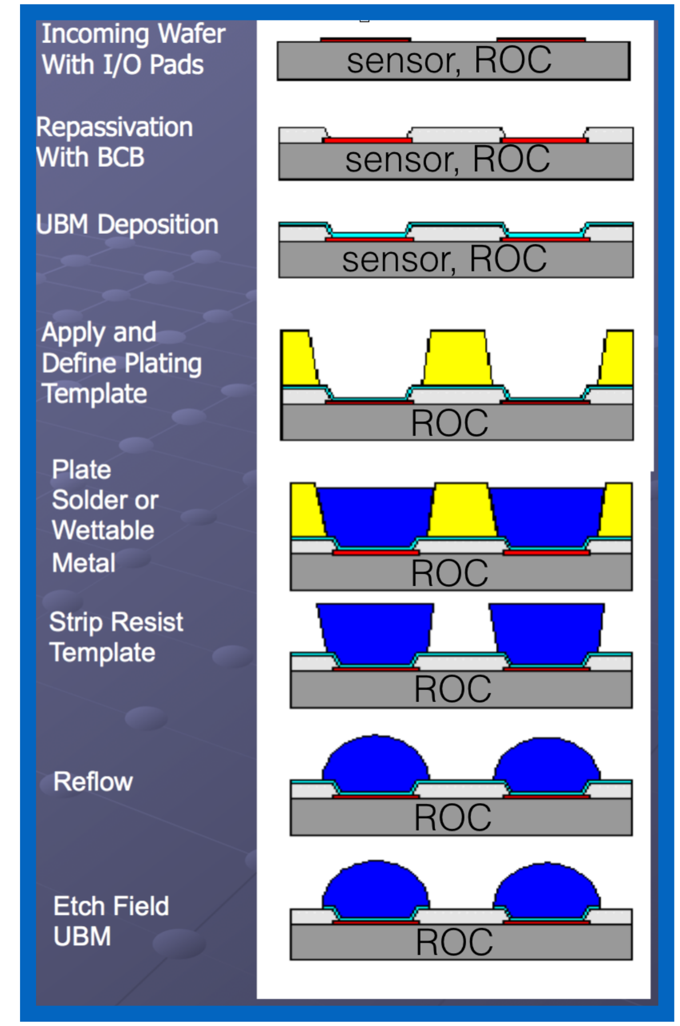
damage is generally from mechanical stress and thus concentrates around the edges of the ROC

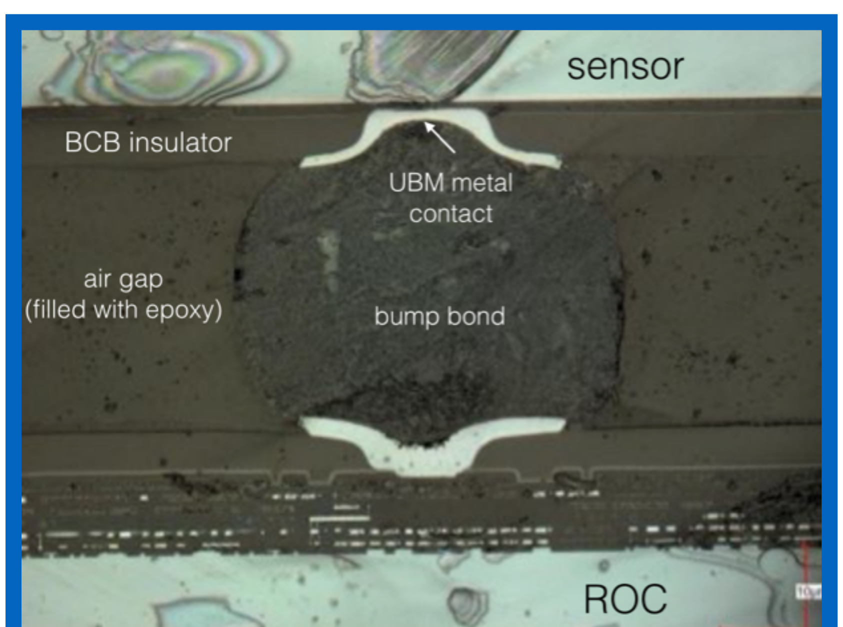
Preproduction “Fingerprint” Issue



pattern correlated over multiple sensors on the original silicon wafer

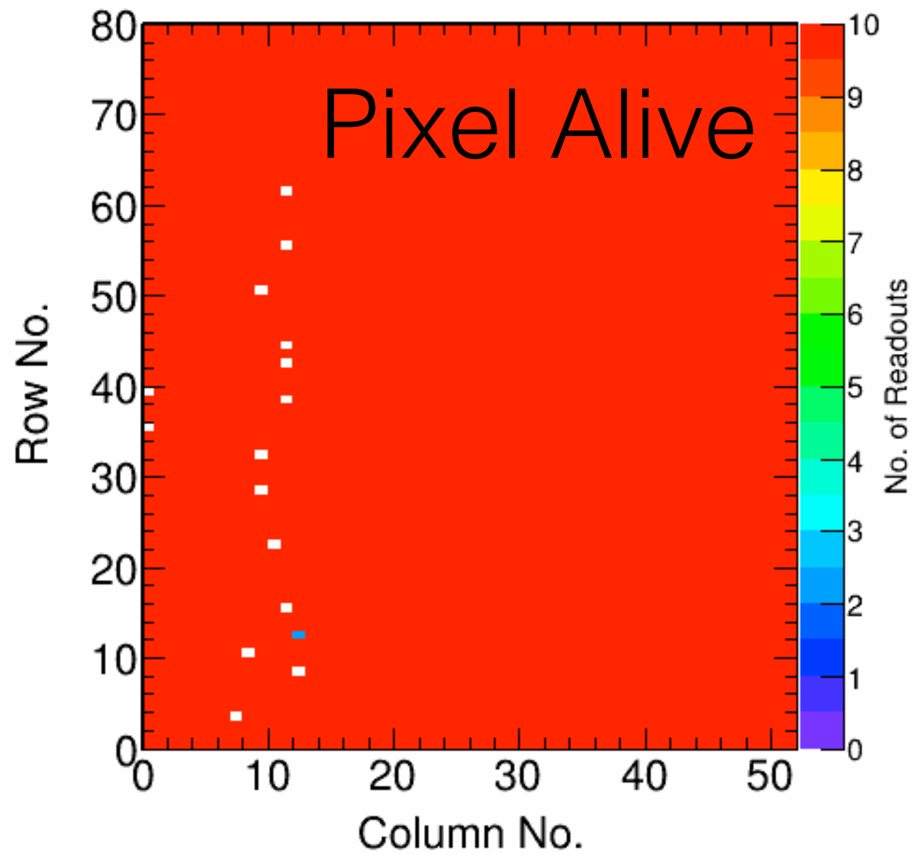
inefficiency in plasma etching of BCB insulating layer between bump bond and sensor surface

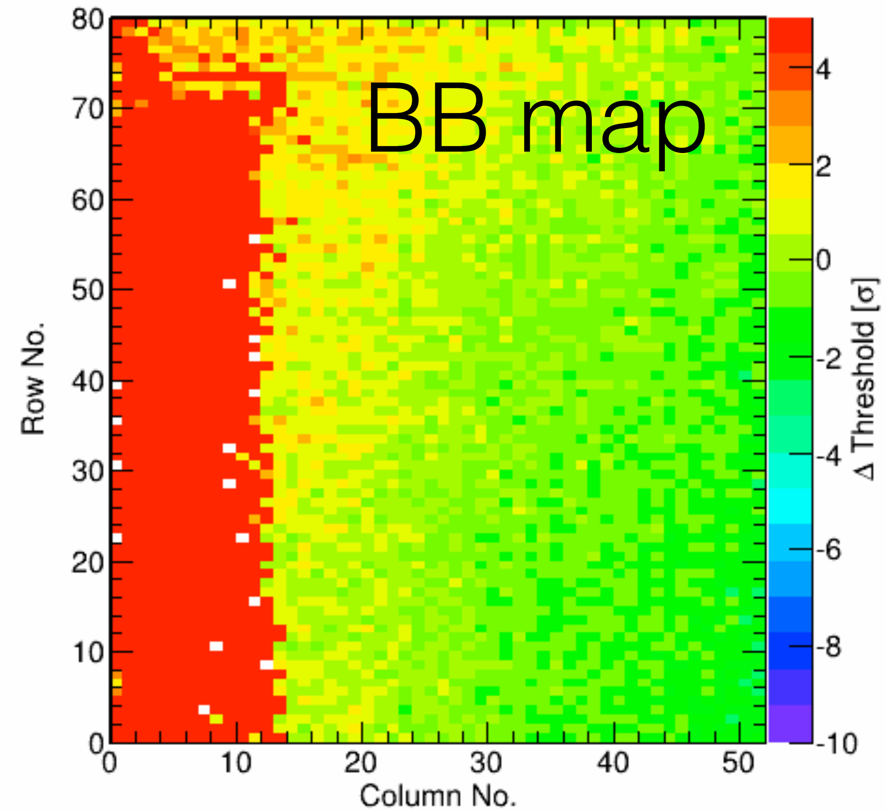


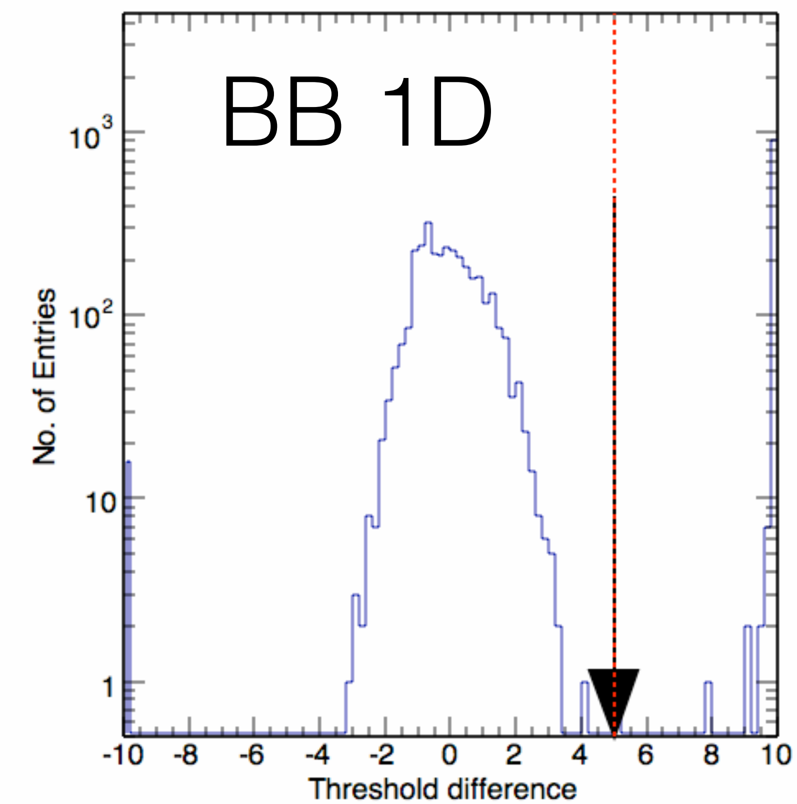


We used variety of tools and expertise, in collaboration with the vendor, to rectify a problem that could have slowed production

Partially detached ROCs







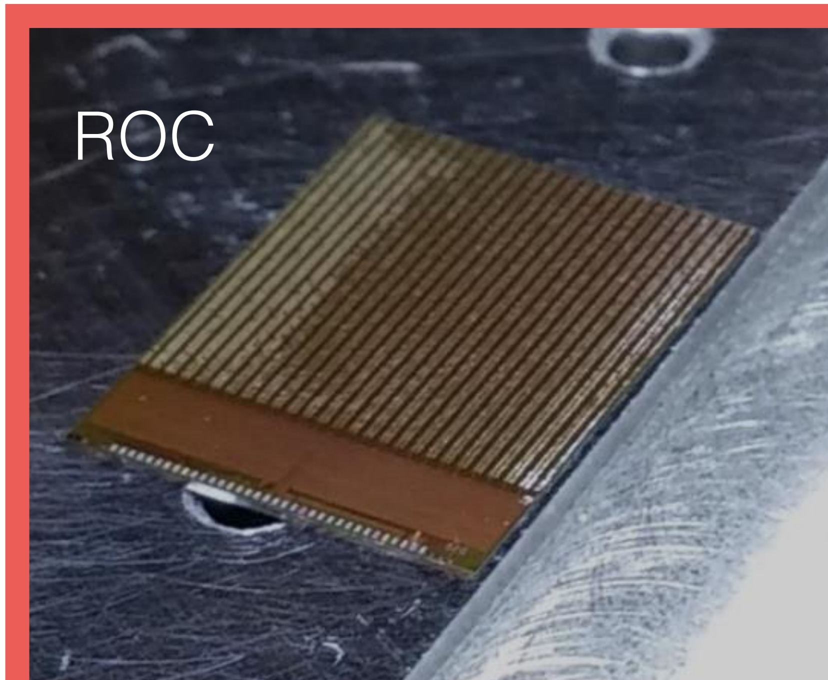
Pattern of dead pixels along a border of regions of working and non-working bump bonds

Working/non-working bumps are well separated in BB discriminant

Size of region of bad bumps varies greatly from module to module

Cause: Misplaced bump bond

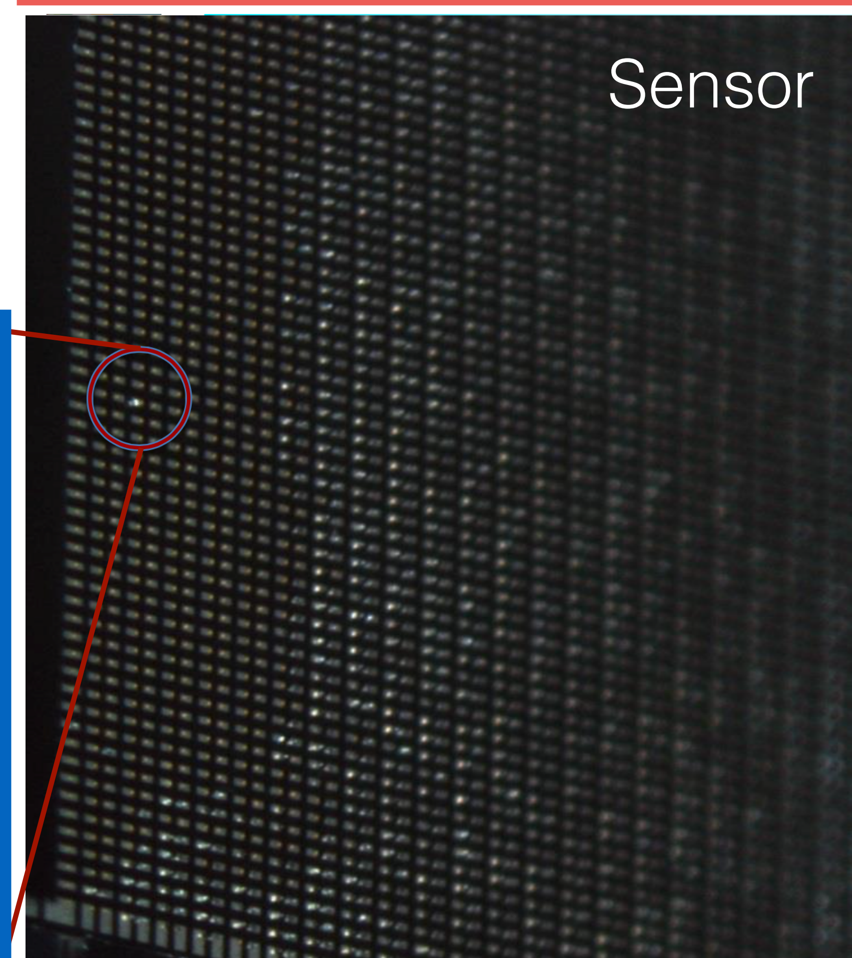
ROC from previous slide was removed from module

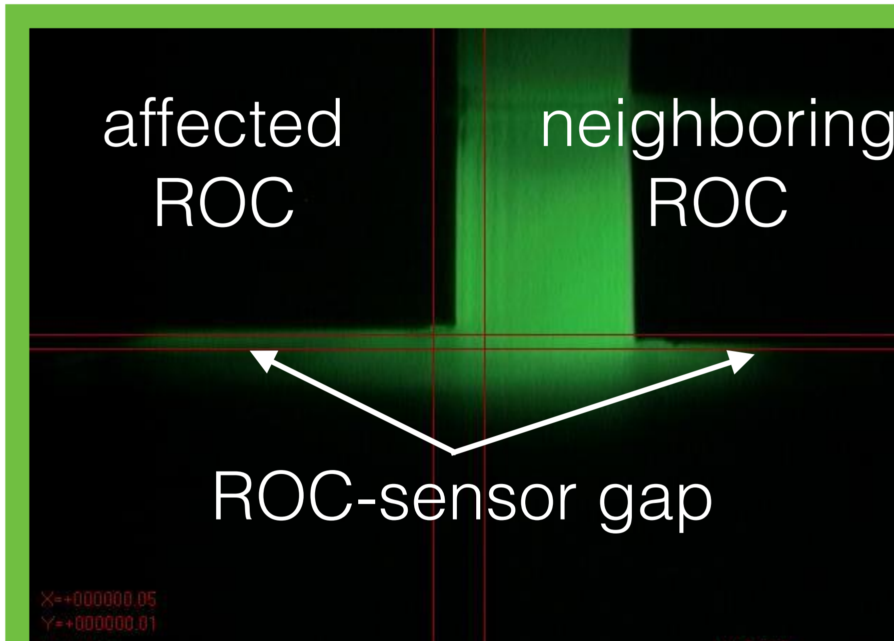


A single misplaced bump bond was observed

Misplaced bump acts as a wedge between sensor and ROC during bump-bonding

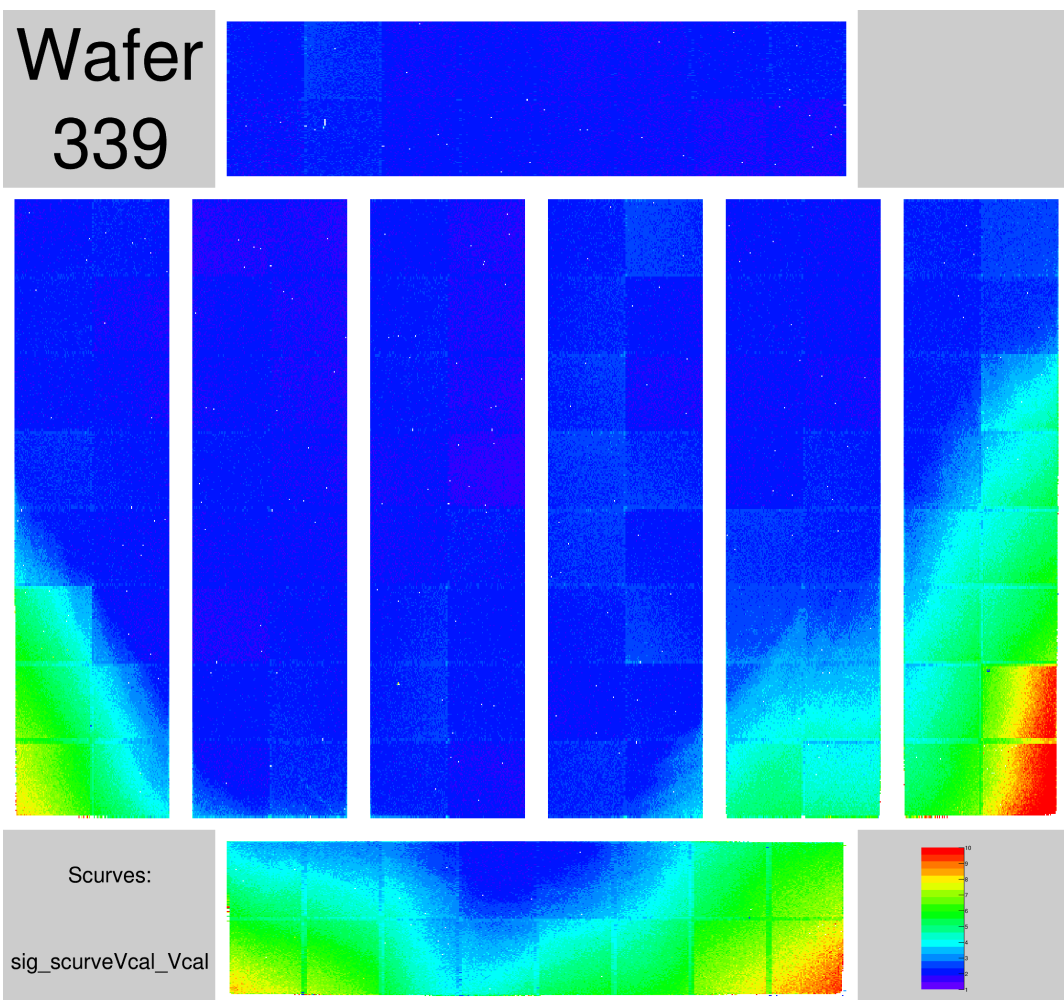
An additional ~10 μm gap was observed between ROC and sensor in one such module



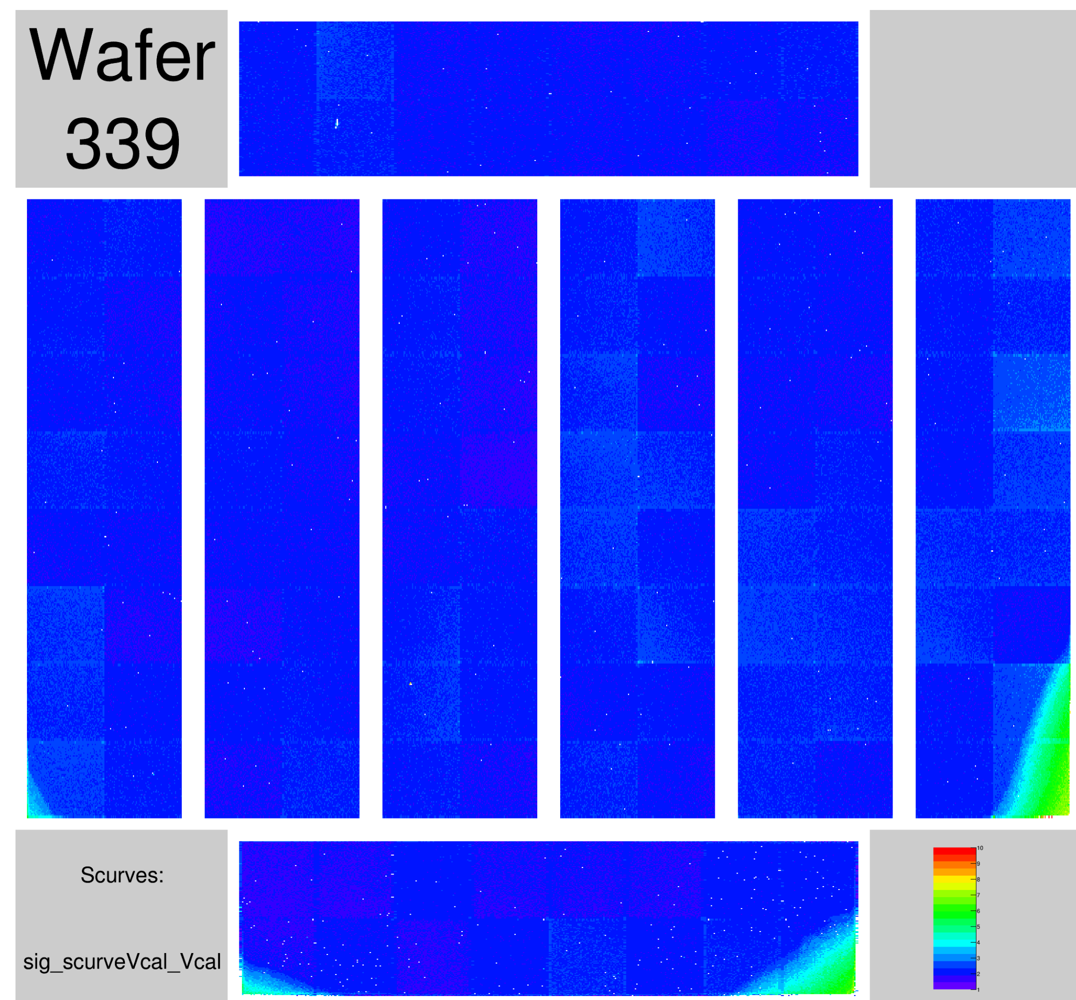


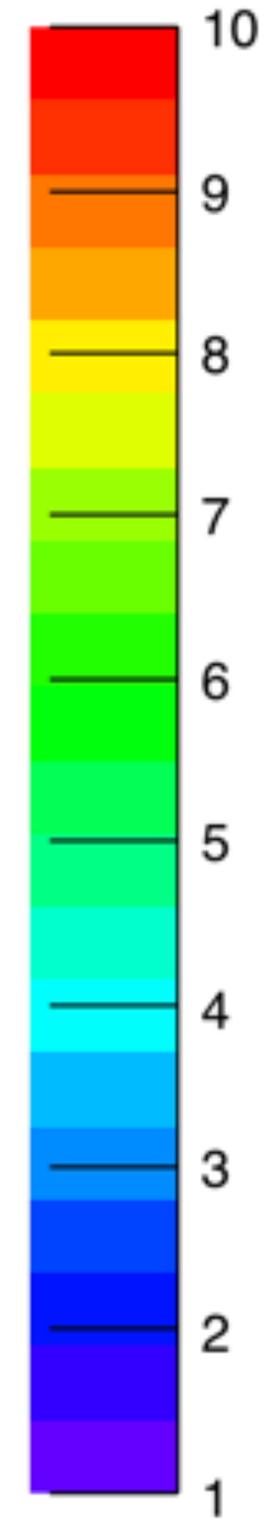
Increasing bias (-330V) reduces noise

bias = -150 V



bias = -330 V





modules could be operated with higher bias,
but must avoid sensor breakdown